

Model Name : GA-G31M-S2C

Revision 1.11

SHEET

TITLE

SHEET

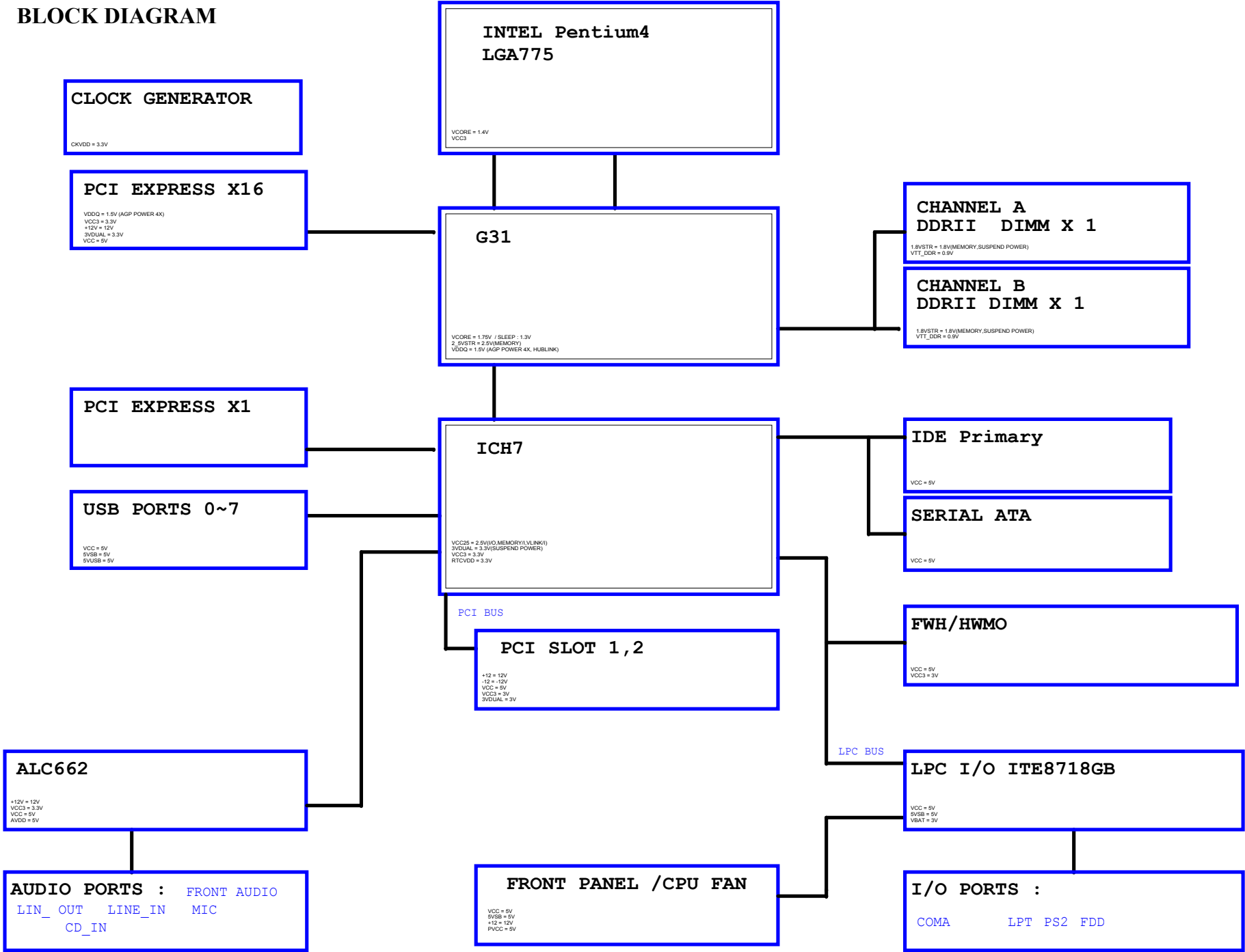
TITLE

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05	P4 LGA775 B,D
06	P4 LGA775 C
07	P4 LGA775 E,F,G,H
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09	G31 DDRII
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20	ICH7 VCC, GND
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23	IDE/FLOPPY
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Gigabyte Technology			
Title Cover Sheet			
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BLOCK DIAGRAM

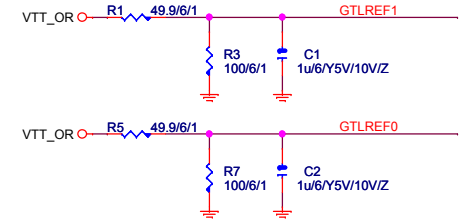
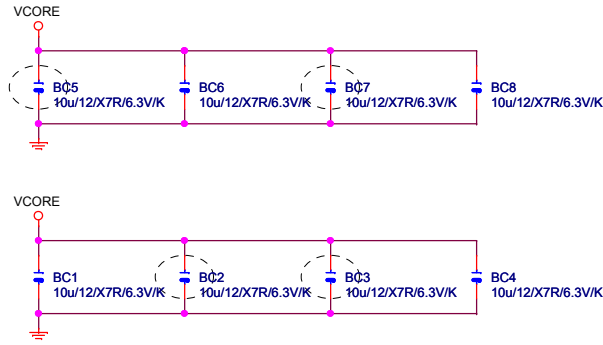


Version: 1.11

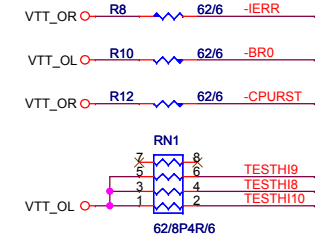
2008/07/18

[illegible][illegible]

<i>Gigabyte Technology</i>			
BOM & PCB MODIFY HISTORY			
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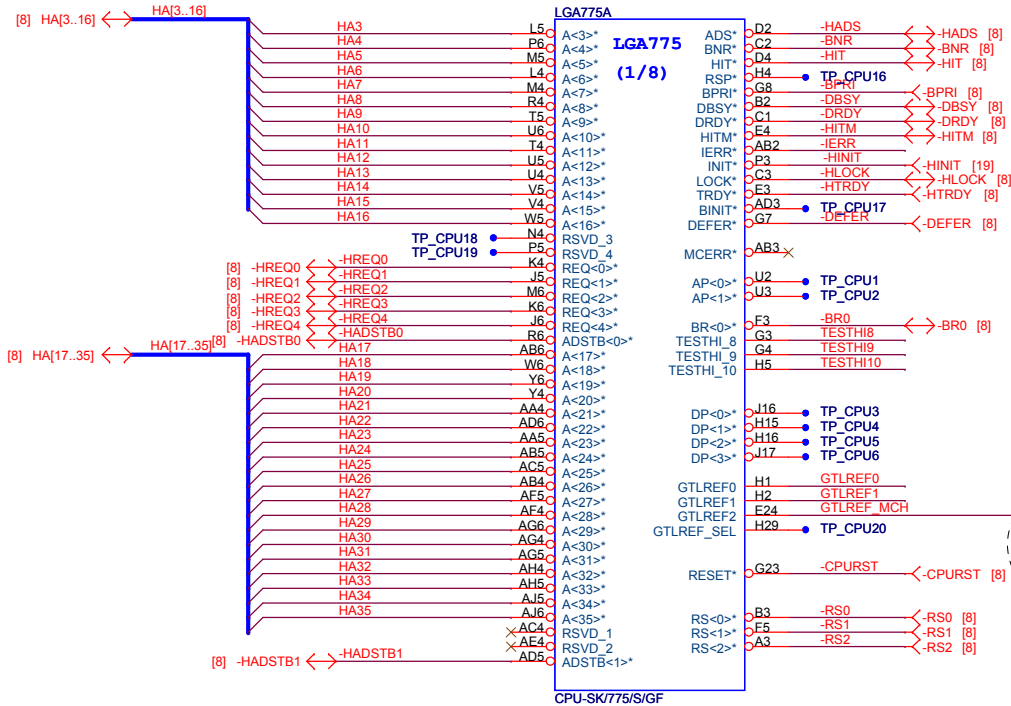
中間値0.9V



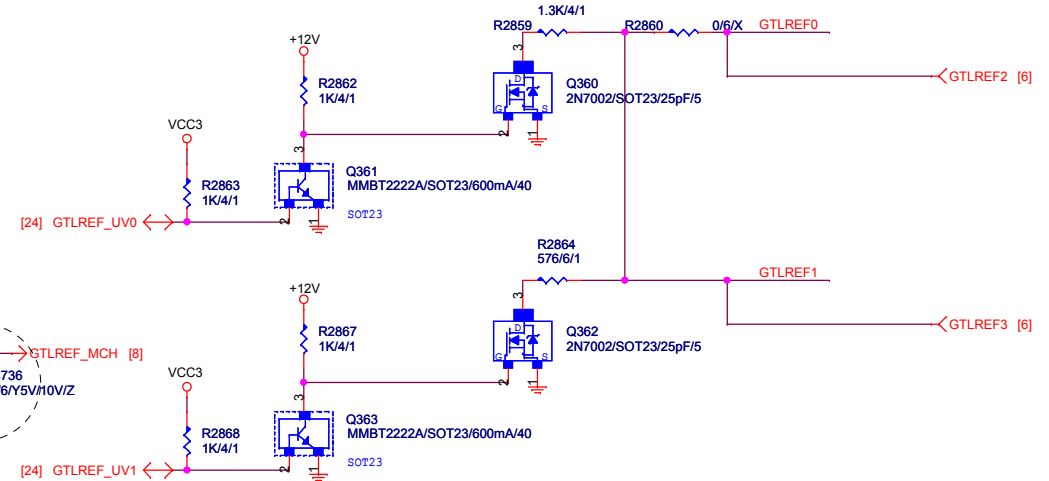
LGA775-39

LGA775A

LGA775
(1/8)

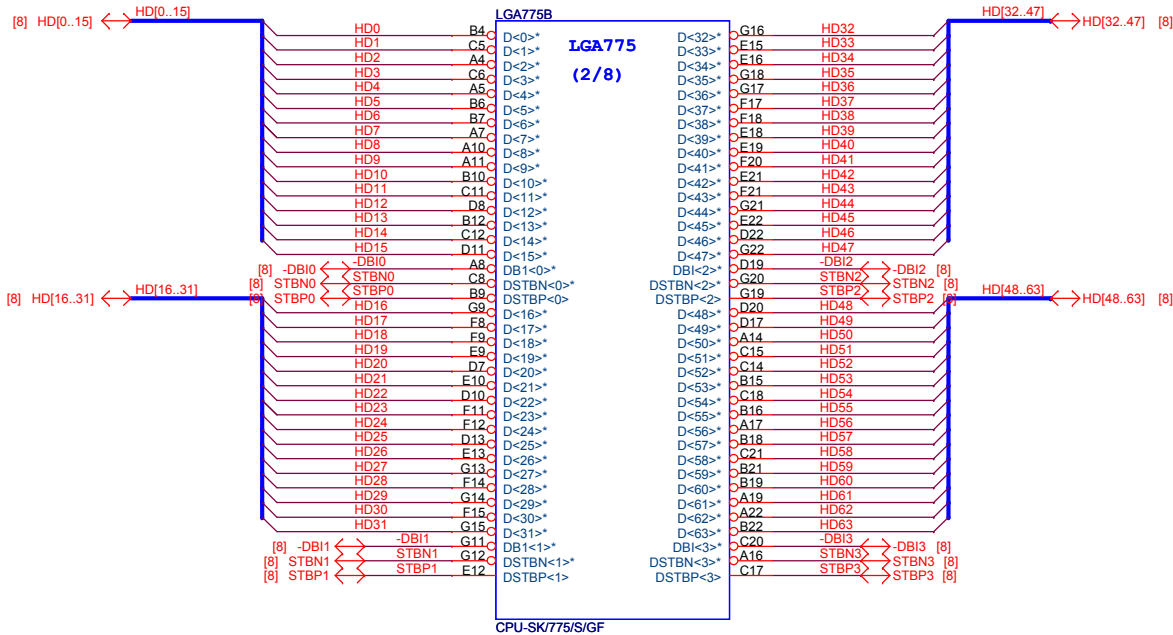


CPU-SK775/S/GF

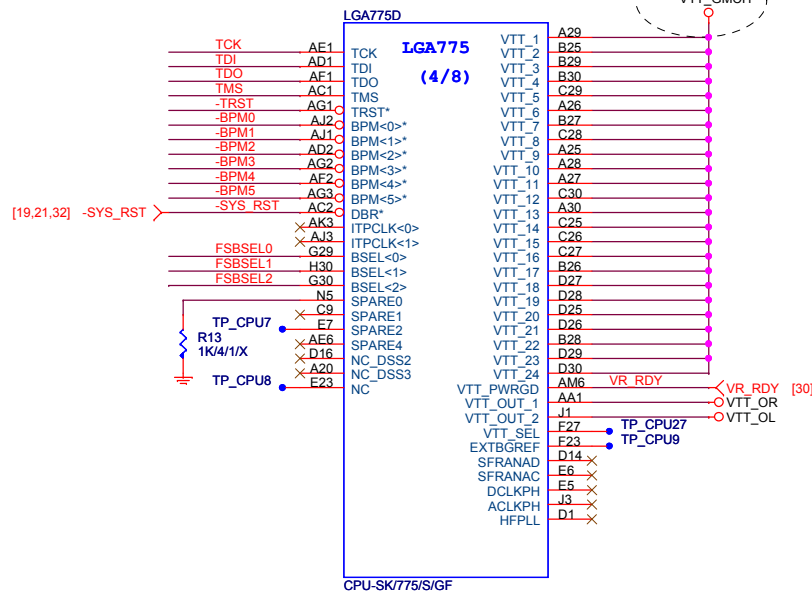


Gigabyte Technology

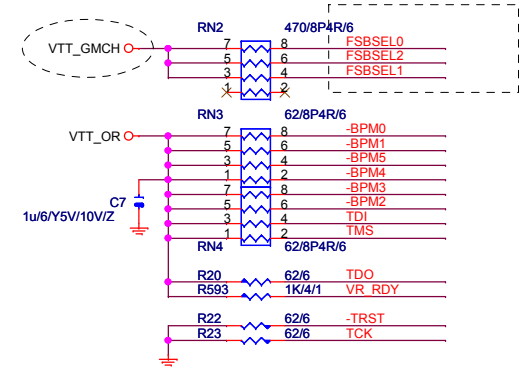
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P4_LGA775-A			
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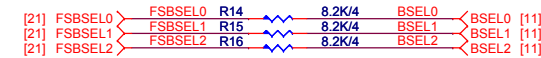
CPU-SK/775/S/GF



CPU-SK/775/S/GF



TO CLK GEN

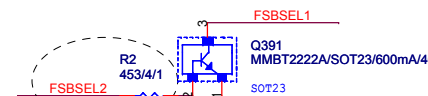


TO NB

CPU

NA	FSB	FSA	
FSBSEL3	FSBSEL1	FSBSEL0	Clock
1	0	1	100MHz
0	0	1	133MHz
0	1	1	166MHz
0	1	0	200MHz
0	0	0	266MHz

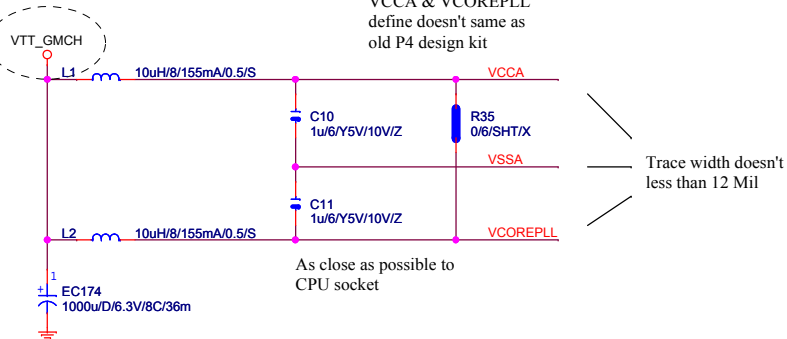
X



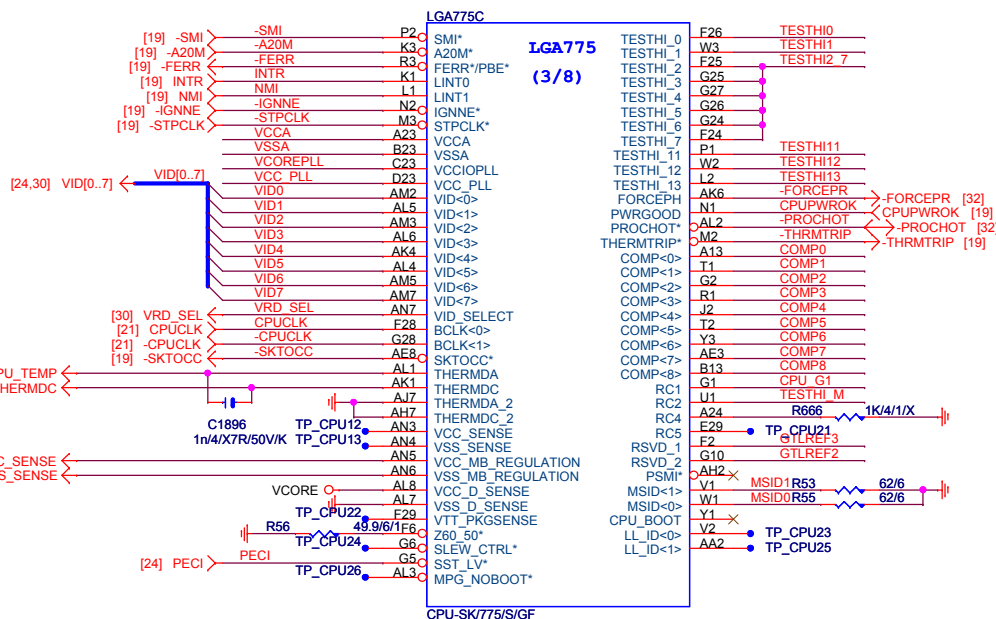
FIX FSB1600 LATCH FAIL

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Title			
P4_LGA775-B,D			
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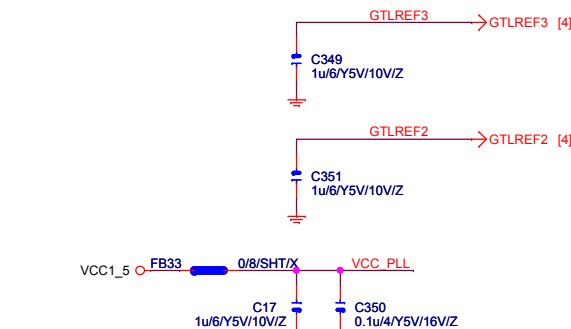
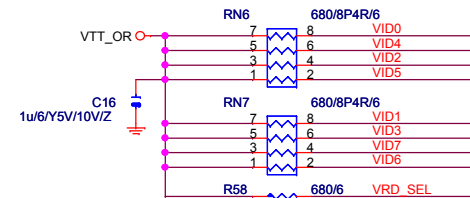
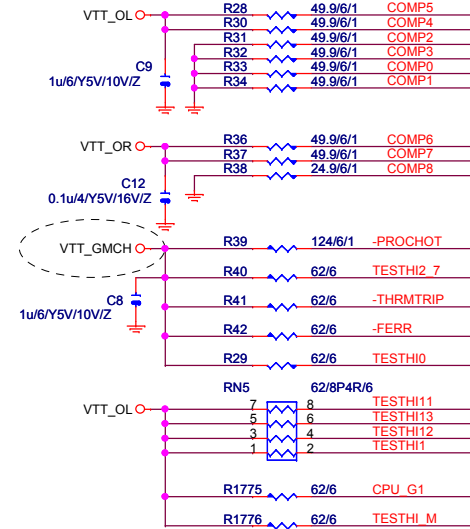
Note:
VCCA & VCOREPLL
define doesn't same as
old P4 design kit



As close as possible to
CPU socket

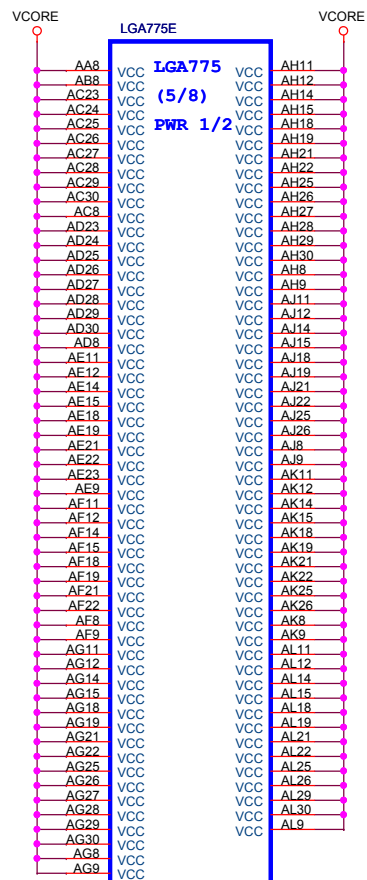


Place outside of CPU socket

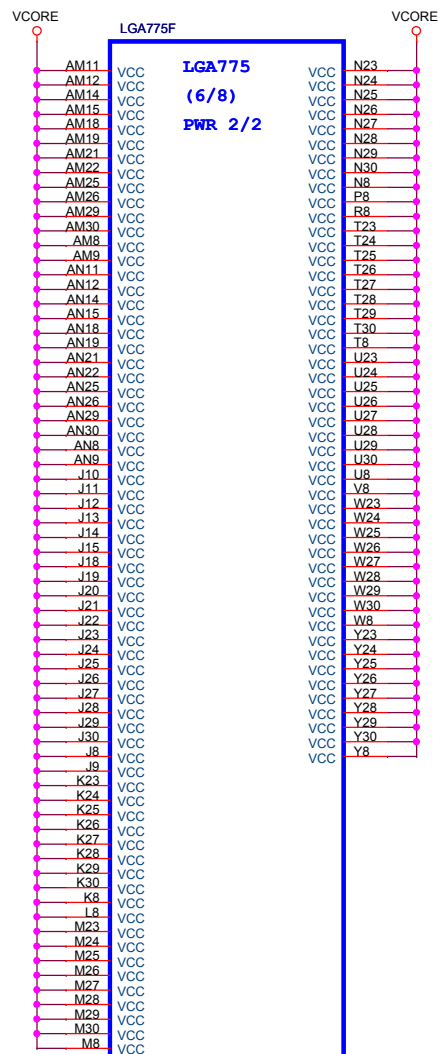


Gigabyte Technology			
Title			
P4_LGA775-C			
Size	Document Number	GA-G31M-S2C	
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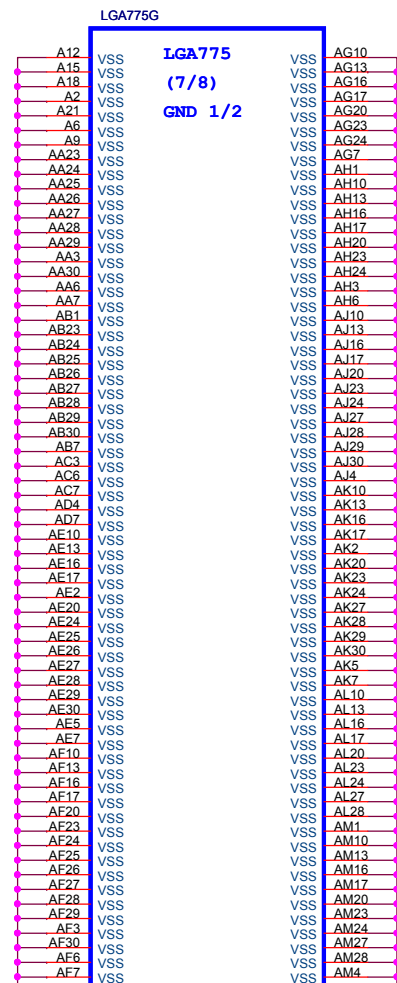
PECI:Platform Environment Control Interface



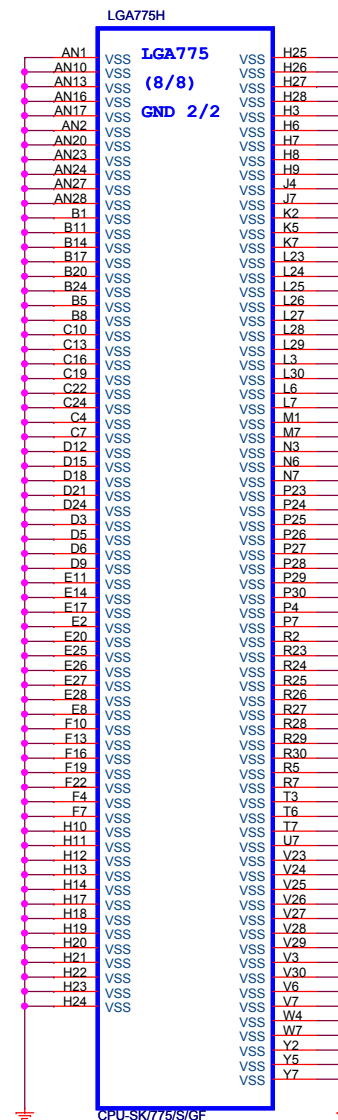
CPU-SK/775/S/GF



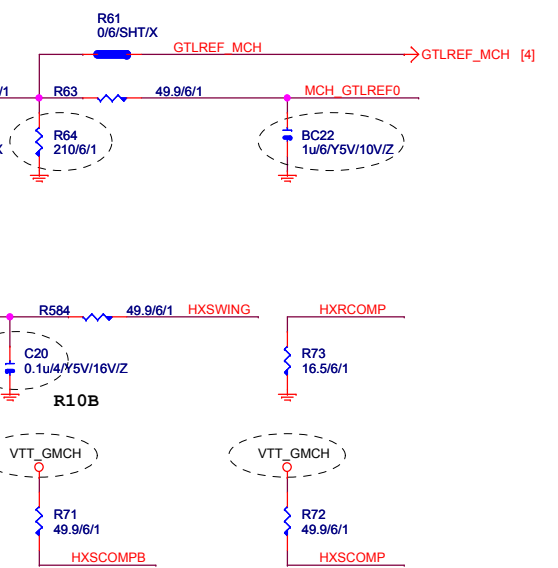
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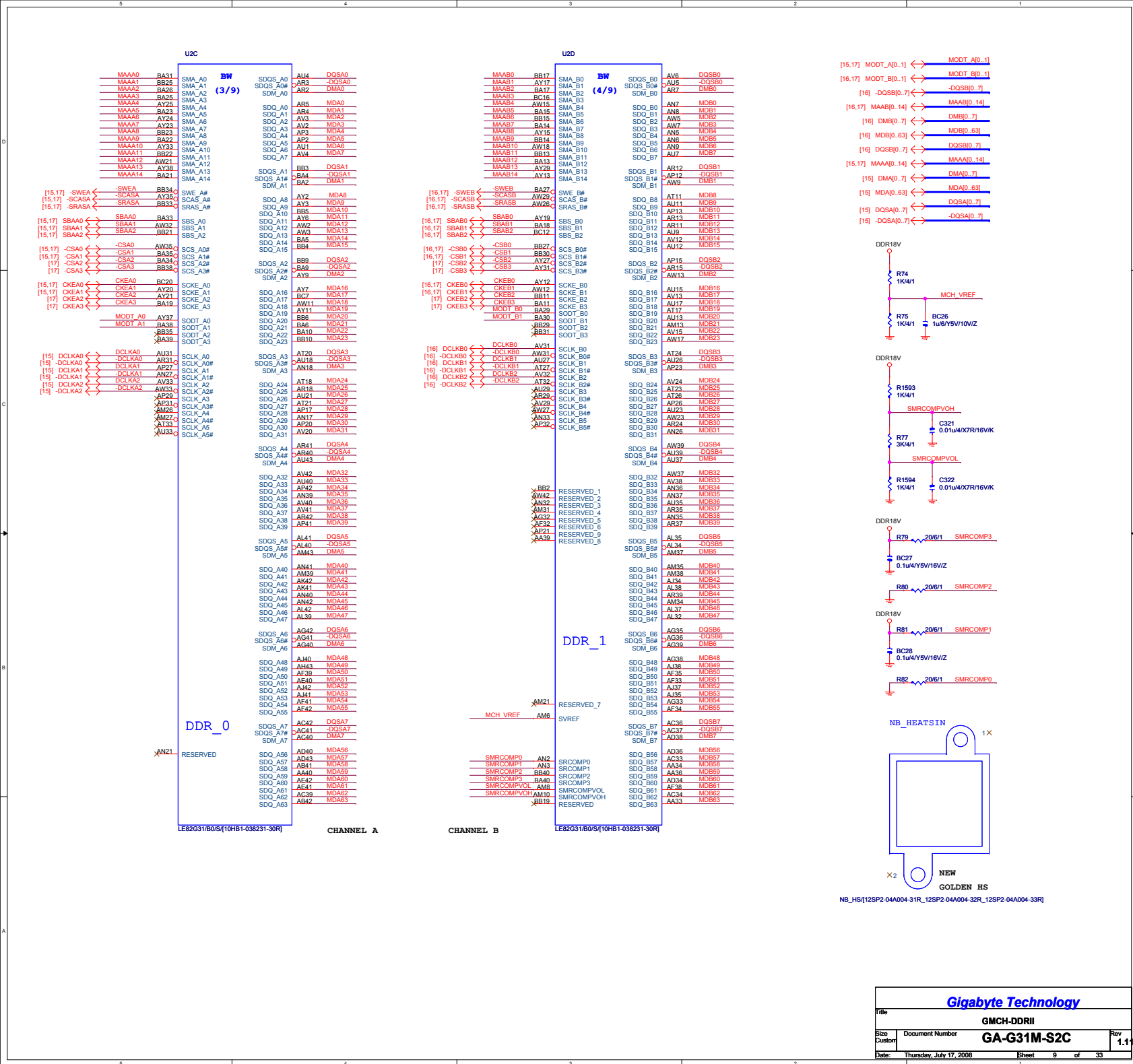


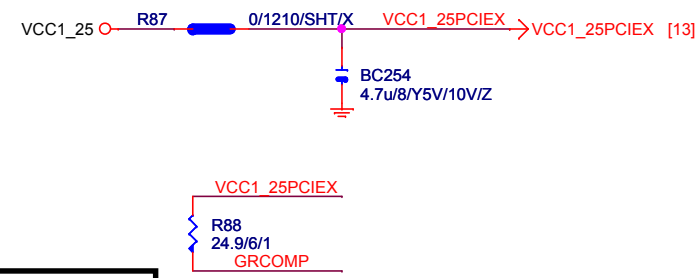
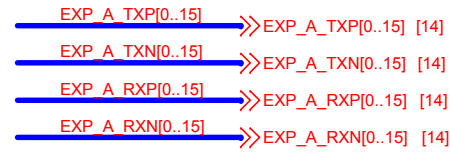
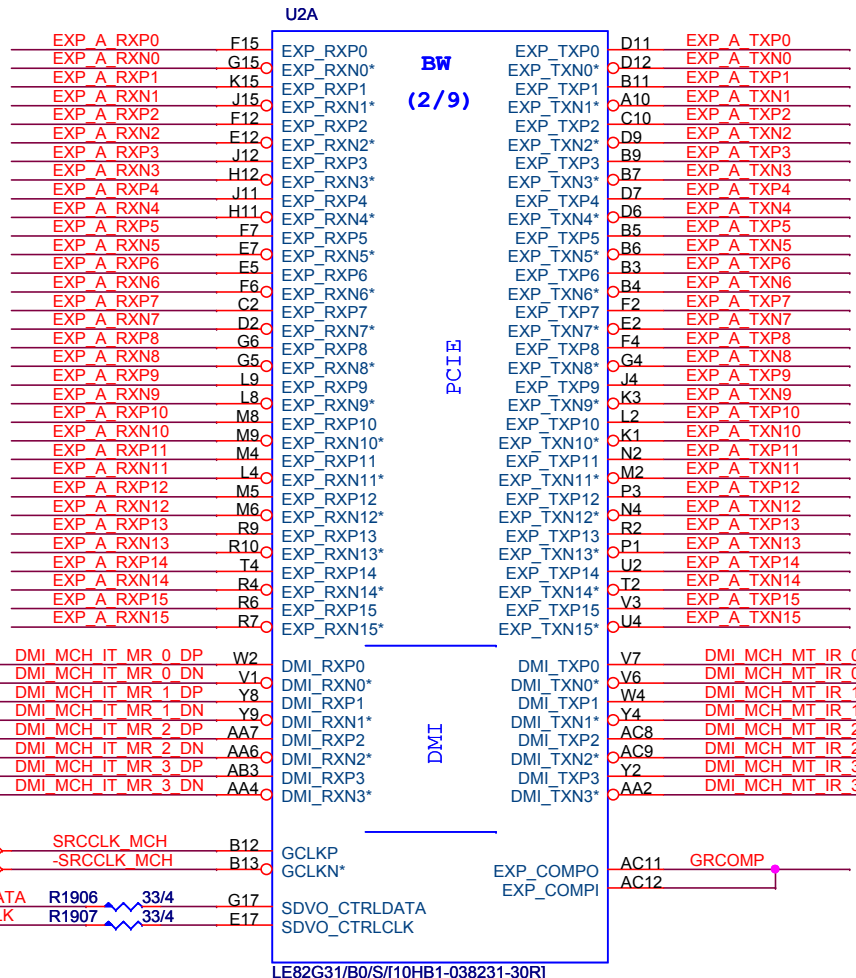
CPU-SK/775/S/GF



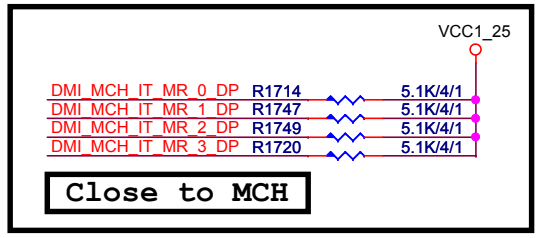
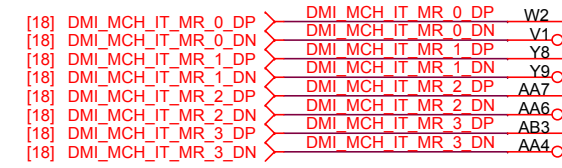
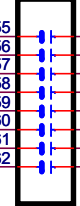
CPU-SK/775/S/GF







Close to MCH

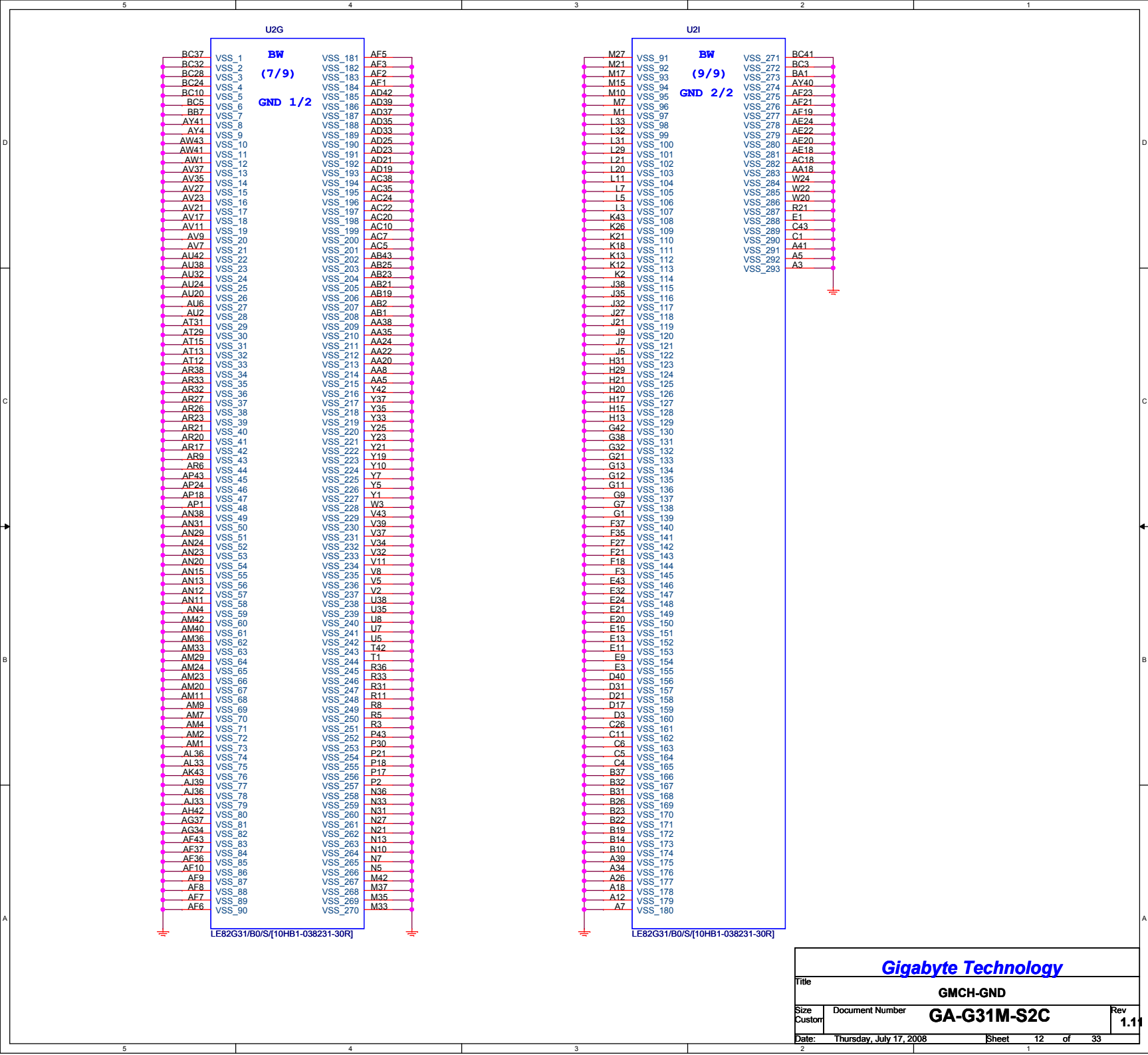


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Gigabyte Technology

Title

GMCH-GND

Size
Custom

Document Number

GA-G31M-S2C

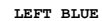
Rev
1.11

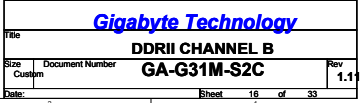
Date: Thursday, July 17, 2008

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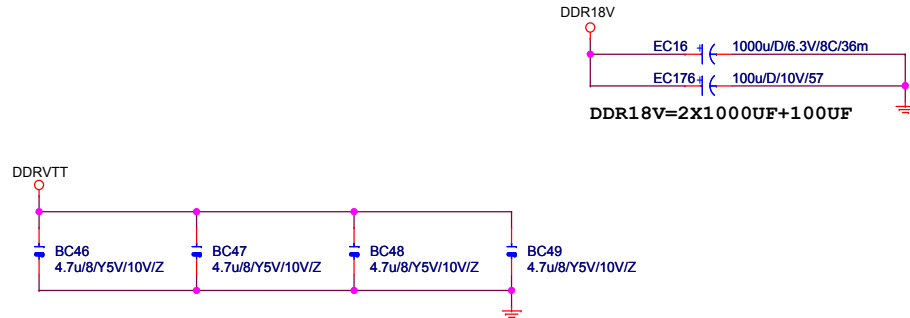
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EXP A TXN0	C93	1.01uW/XTR/16V/K	EXP A TXN0C
EXP A TXP1	C94	1.01uW/XTR/16V/K	EXP A TXP1C
EXP A TXN1	C95	1.01uW/XTR/16V/K	EXP A TXN1C
EXP A TPX2	C96	1.01uW/XTR/16V/K	EXP A TPX2C
EXP A TXN2	C97	1.01uW/XTR/16V/K	EXP A TXN2C
EXP A TPX3	C98	1.01uW/XTR/16V/K	EXP A TPX3C
EXP A TXN3	C99	1.01uW/XTR/16V/K	EXP A TXN3C
EXP A TPX4	C100	1.01uW/XTR/16V/K	EXP A TPX4C
EXP A TXN4	C101	1.01uW/XTR/16V/K	EXP A TXN4C
EXP A TPX5	C102	1.01uW/XTR/16V/K	EXP A TPX5C
EXP A TXN5	C103	1.01uW/XTR/16V/K	EXP A TXN5C
EXP A TPX6	C104	1.01uW/XTR/16V/K	EXP A TPX6C
EXP A TXN6	C105	1.01uW/XTR/16V/K	EXP A TXN6C
EXP A TPX7	C106	1.01uW/XTR/16V/K	EXP A TPX7C
EXP A TXN7	C107	1.01uW/XTR/16V/K	EXP A TXN7C
EXP A TPX8	C108	1.01uW/XTR/16V/K	EXP A TPX8C
EXP A TXN8	C109	1.01uW/XTR/16V/K	EXP A TXN8C
EXP A TPX9	C110	1.01uW/XTR/16V/K	EXP A TPX9C
EXP A TXN9	C111	1.01uW/XTR/16V/K	EXP A TXN9C
EXP A TPX10	C112	1.01uW/XTR/16V/K	EXP A TPX10C
EXP A TXN10	C113	1.01uW/XTR/16V/K	EXP A TXN10C
EXP A TPX11	C114	1.01uW/XTR/16V/K	EXP A TPX11C
EXP A TXN11	C115	1.01uW/XTR/16V/K	EXP A TXN11C
EXP A TPX12	C116	1.01uW/XTR/16V/K	EXP A TPX12C
EXP A TXN12	C117	1.01uW/XTR/16V/K	EXP A TXN12C
EXP A TPX13	C118	1.01uW/XTR/16V/K	EXP A TPX13C
EXP A TXN13	C119	1.01uW/XTR/16V/K	EXP A TXN13C
EXP A TPX14	C120	1.01uW/XTR/16V/K	EXP A TPX14C
EXP A TXN14	C121	1.01uW/XTR/16V/K	EXP A TXN14C
EXP A TPX15	C122	1.01uW/XTR/16V/K	EXP A TPX15C
EXP A TXN15	C123	1.01uW/XTR/16V/K	EXP A TXN15C



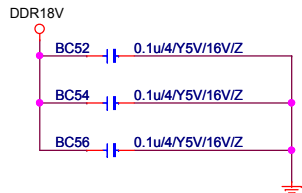


DDR TERMINATION CHANNEL A

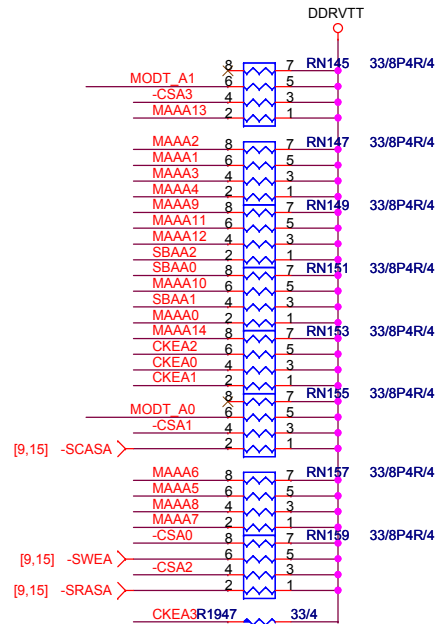
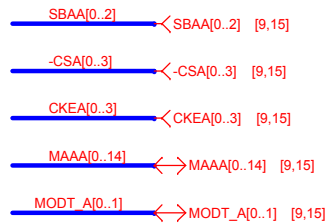
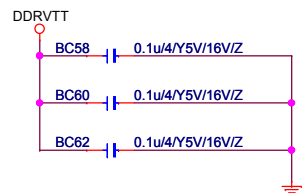
DDRVTT Decouple



DDR18V Decouple

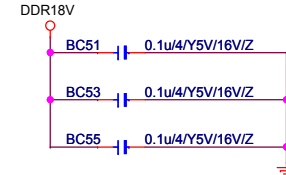


DDRVTT Decouple

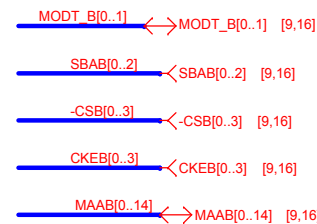
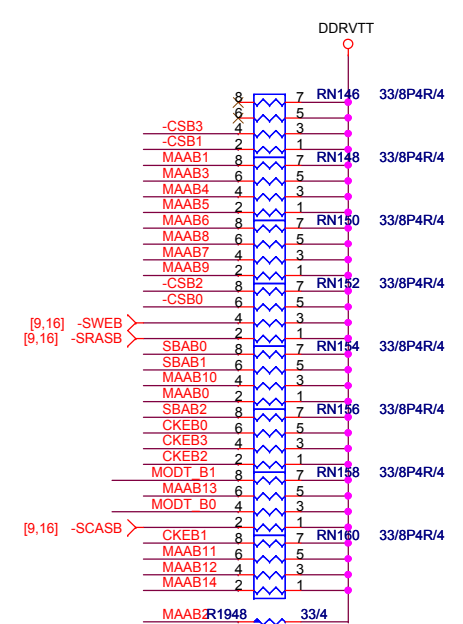
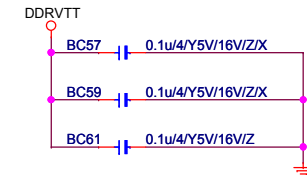


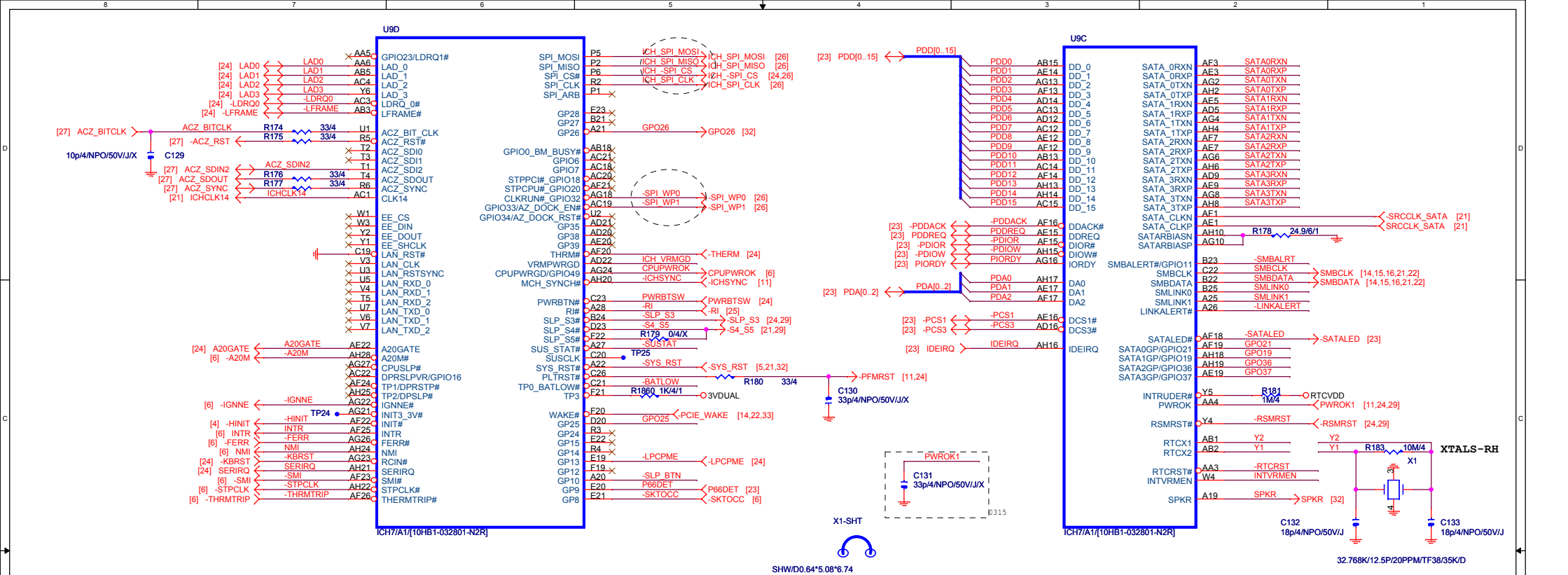
DDR TERMINATION CHANNEL B

DDR18V Decouple



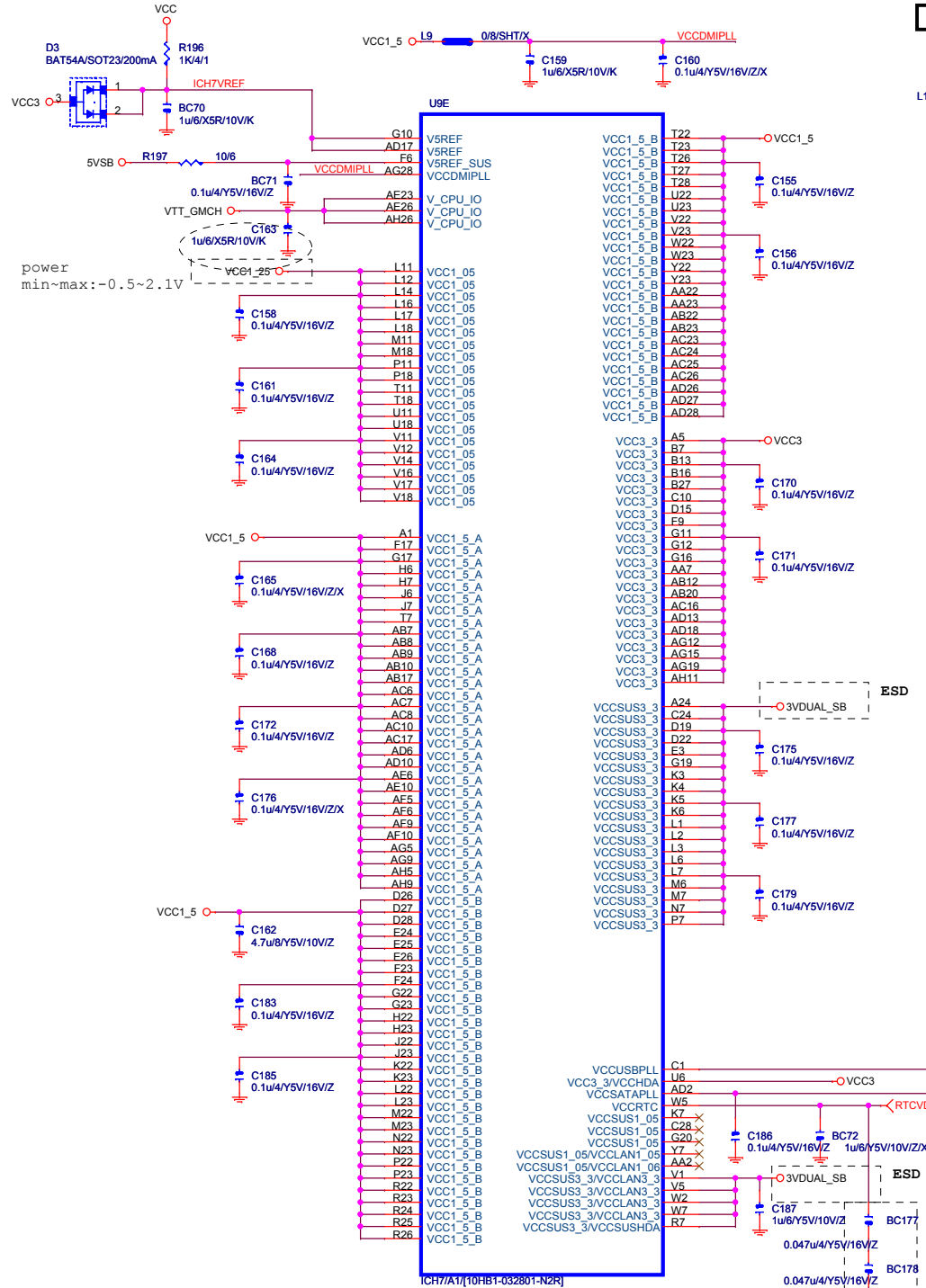
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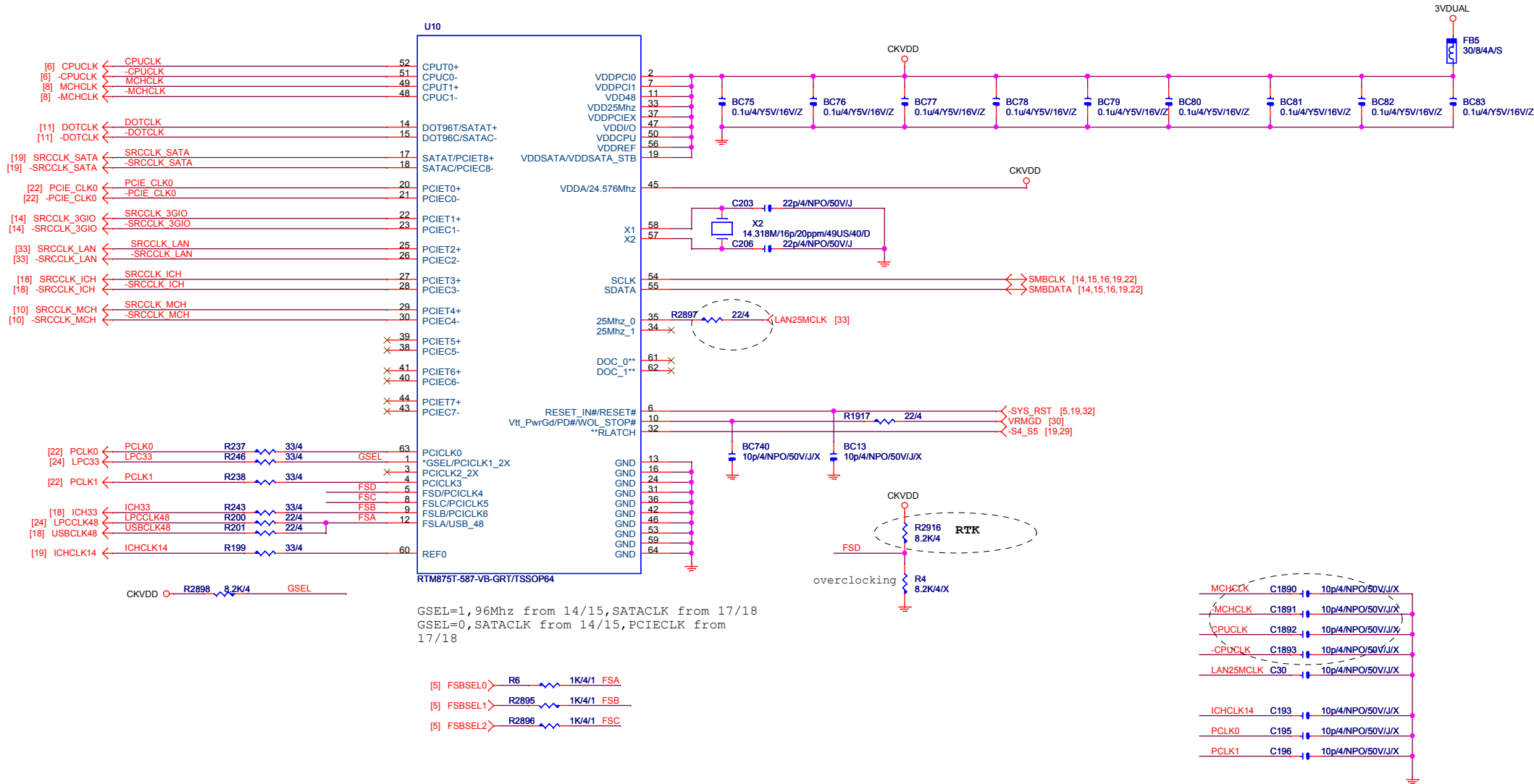




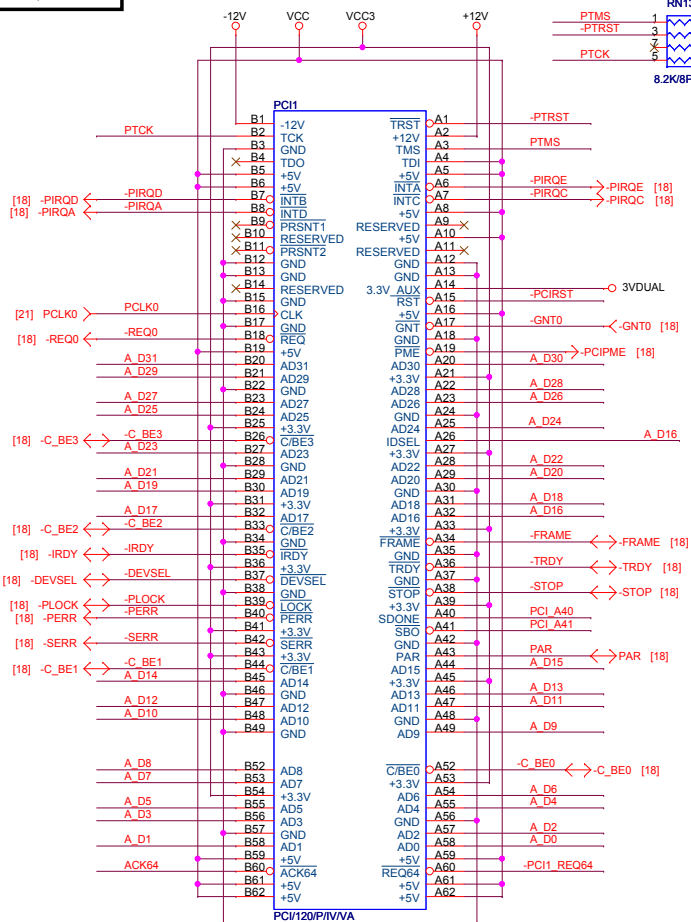
U9F		
A4	VSS1	VSS101
A23	VSS2	VSS102
B1	VSS3	VSS103
B8	VSS4	VSS104
B11	VSS5	VSS105
B14	VSS6	VSS106
B17	VSS7	VSS107
B20	VSS8	VSS108
B26	VSS9	VSS109
B28	VSS10	VSS110
C2	VSS11	VSS111
C6	VSS12	VSS112
D10	VSS13	VSS113
D13	VSS14	VSS114
D18	VSS15	VSS115
D21	VSS16	VSS116
D24	VSS17	VSS117
E1	VSS18	VSS118
E2	VSS19	VSS119
E8	VSS20	VSS120
E15	VSS21	VSS121
F3	VSS22	VSS122
F4	VSS23	VSS123
F5	VSS24	VSS124
F12	VSS25	VSS125
F27	VSS26	VSS126
F28	VSS27	VSS127
G1	VSS28	VSS128
G2	VSS29	VSS129
G5	VSS30	VSS130
G6	VSS31	VSS131
G9	VSS32	VSS132
G14	VSS33	VSS133
G18	VSS34	VSS134
G21	VSS35	VSS135
G24	VSS36	VSS136
G25	VSS37	VSS137
G26	VSS38	VSS138
H3	VSS39	VSS139
H4	VSS40	VSS140
H5	VSS41	VSS141
H24	VSS42	VSS142
H27	VSS43	VSS143
H28	VSS44	VSS144
J1	VSS45	VSS145
J5	VSS46	VSS146
J24	VSS47	VSS147
J25	VSS48	VSS148
J26	VSS49	VSS149
J26	VSS50	VSS150
K24	VSS51	VSS151
K27	VSS52	VSS152
K28	VSS53	VSS153
L13	VSS54	VSS154
L15	VSS55	VSS155
L24	VSS56	VSS156
L25	VSS57	VSS157
L26	VSS58	VSS158
M3	VSS59	VSS159
M4	VSS60	VSS160
M5	VSS61	VSS161
M12	VSS62	VSS162
M13	VSS63	VSS163
M14	VSS64	VSS164
M15	VSS65	VSS165
M16	VSS66	VSS166
M17	VSS67	VSS167
M24	VSS68	VSS168
M27	VSS69	VSS169
M28	VSS70	VSS170
N1	VSS71	VSS171
N2	VSS72	VSS172
N5	VSS73	VSS173
N6	VSS74	VSS174
N11	VSS75	VSS175
N12	VSS76	VSS176
N13	VSS77	VSS177
N14	VSS78	VSS178
N15	VSS79	VSS179
N16	VSS80	VSS180
N17	VSS81	VSS181
N18	VSS82	VSS182
N24	VSS83	VSS183
N25	VSS84	VSS184
N26	VSS85	VSS185
P3	VSS86	VSS186
P4	VSS87	VSS187
P12	VSS88	VSS188
P13	VSS89	VSS189
P14	VSS90	VSS190
P15	VSS91	VSS191
P16	VSS92	VSS192
P17	VSS93	VSS193
P24	VSS94	VSS194
P27	VSS95	
P28	VSS96	
R1	VSS97	
R11	VSS98	
R12	VSS99	
R13	VSS100	

ICH7/A1/[10HB1-032801-N2R]

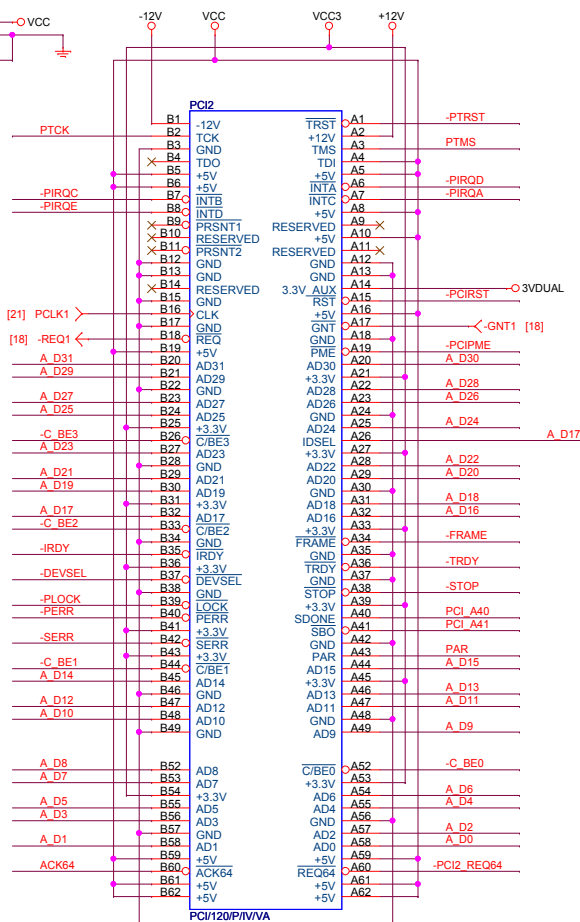
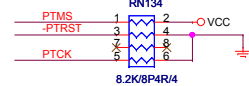




PCI1,2 SLOT

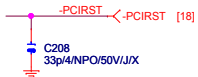
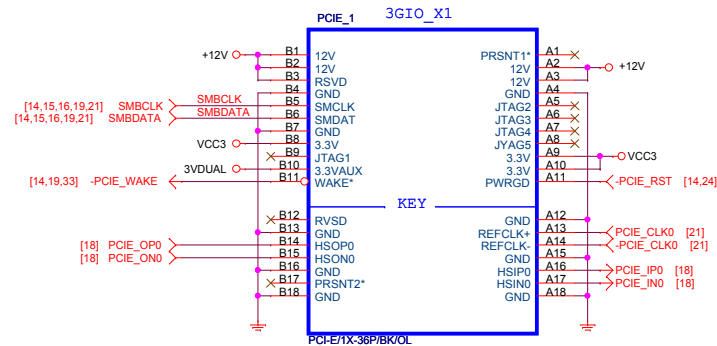


AD_16/-PIRQ(E-D-C-A)/-REQ0/-GNT0

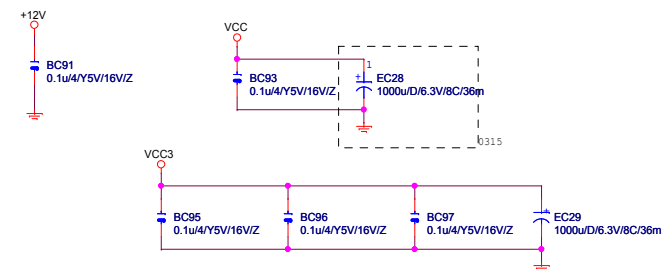
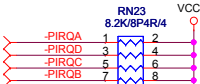
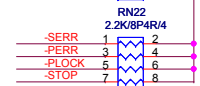
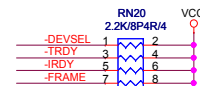
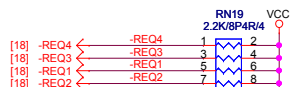


AD_17/-PIRQ(D-C-A-E)/-REQ1/-GNT1

PCIE*1



Place close to PCI1



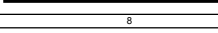
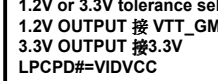
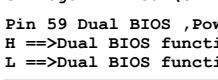
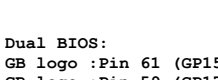
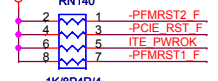
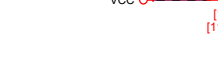
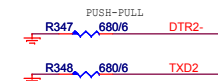
The schematic diagram illustrates the internal components of the USB1 module. On the left, the 'FRONT USB1' view shows the connection of USB signals to the ESD1 protection diode array (CM1293-04SO/SO23-6) and the BC780 fuse (0.1u/4Y5V/16V/Z). The right side shows the 'FUSEVCC1' view, detailing the connection of the fuse to the F_USB1 fuse block (PHI2*5K9/YL/2.5A/VA/D) and the FUSEVCC1 supply.

The schematic diagram illustrates the USB to RS-485 converter circuit. It features a 5V DUAL input connected to two diodes, F1 and F2, both labeled SMD1812P260/6V. Diode F1 is connected to FUSEVCC, and diode F2 is connected to FUSEVCC1. Both FUSEVCC and FUSEVCC1 are connected to BC105 and BC714 transistors, respectively, which are labeled 0.1uA/Y5V/16V/Z/X. The circuit also includes resistors R321 (150K/4) and R322 (270K/4). The output is labeled USB_F [18].

The schematic diagram illustrates the USB to SPDIF conversion circuit. The USB connector (USB_RCA) is connected to the SPDIF output. The circuit includes a BC737 optocoupler and several passive components (resistors and capacitors) for signal conditioning. The USB connector pins are labeled U1 through U8, G, G1 through G6. The SPDIF output is labeled SPDIF. The circuit is powered by FUSEVCC and ground.

RTS2- ==LOW CPU FAN 50%
==HIGH 100%

DEFAULT 50%



Dual BIOS:

GB logo :Pin 61 (GP15/CSA)

GB logo :Pin 59 (GP17/CSB)

Pin 59 Dual BIOS ,Power On Strapping:

H ==>Dual BIOS function Enable

L ==>Dual BIOS function Disable

1.2V or 3.3V tolerance select.

1.2V OUTPUT 接 VTT_GMCH

3.3V OUTPUT 接 3.3V

LPCPD# =VIDVCC

Pop to disable Dual BIOS

-SIO_SPI_CS0 R389 0/4 ICH_SPI_CS

-SIO_SPI_CS1 0/4X R412 CEB_N

-SIO_SPI_CS0 0/4X R404 -RST_BTN

-SIO_SPI_CS0 0/4X R404 -RST_BTN

-SIO_SPI_CS0 0/4X R404 -RST_BTN

-SIO_SPI_CS0 0/4X R404 -RST_BTN

-SIO_SPI_CS0 0/4X R404 -RST_BTN

-SIO_SPI_CS0 0/4X R404 -RST_BTN

-SIO_SPI_CS0 0/4X R404 -RST_BTN

-SIO_SPI_CS0 0/4X R404 -RST_BTN

-SIO_SPI_CS0 0/4X R404 -RST_BTN

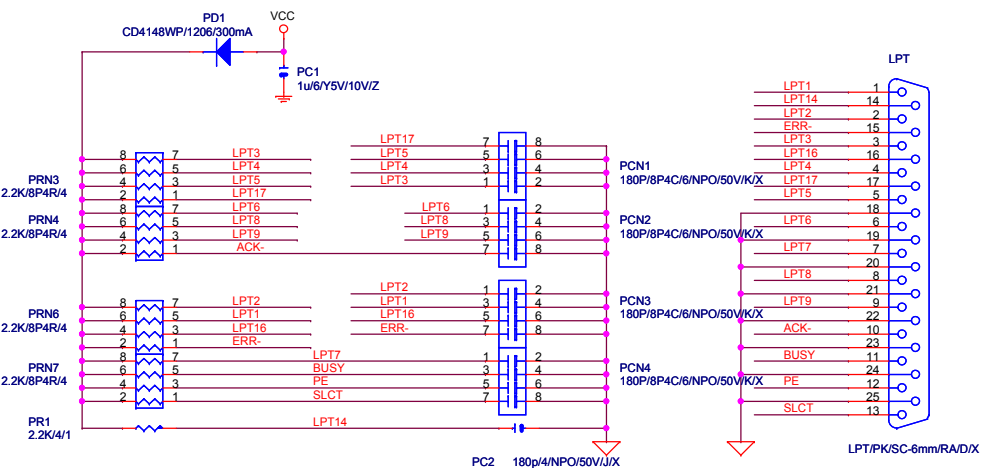
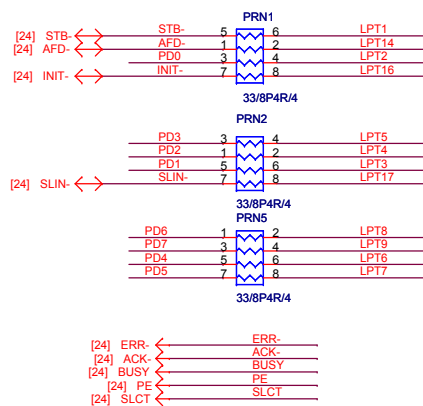
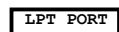
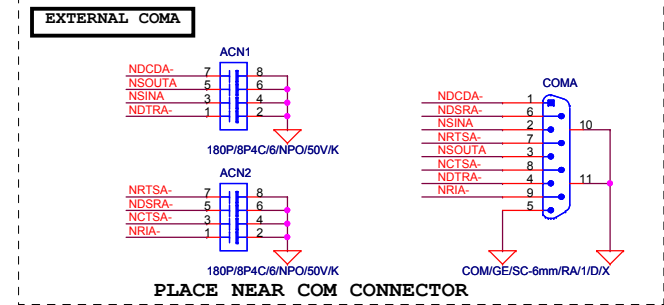
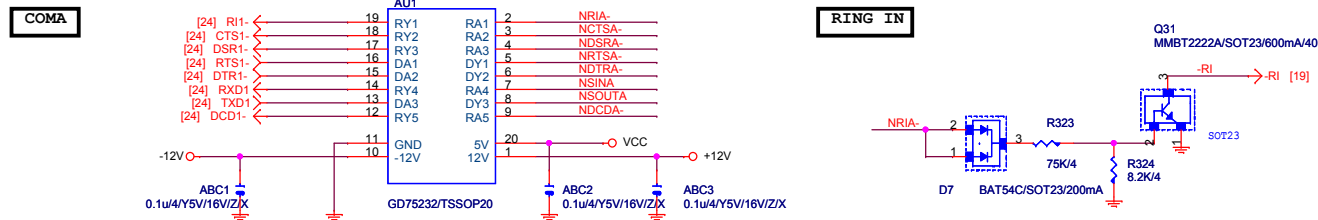
-SIO_SPI_CS0 0/4X R404 -RST_BTN

-SIO_SPI_CS0 0/4X R404 -RST_BTN

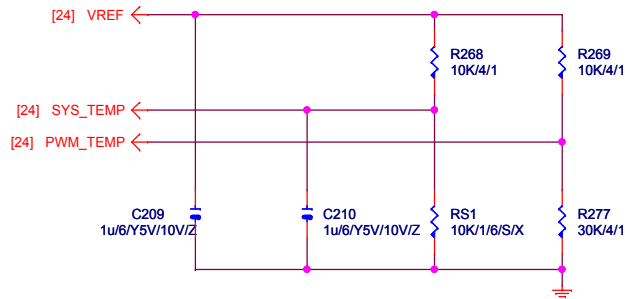
Gigabyte Technology

Title			ITE 8712/18 LPC IO
Size B	Document Number	GA-G31M-S2C	
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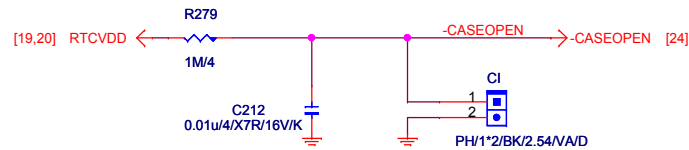
Rev 1.11



TEMP H/W MONITOR

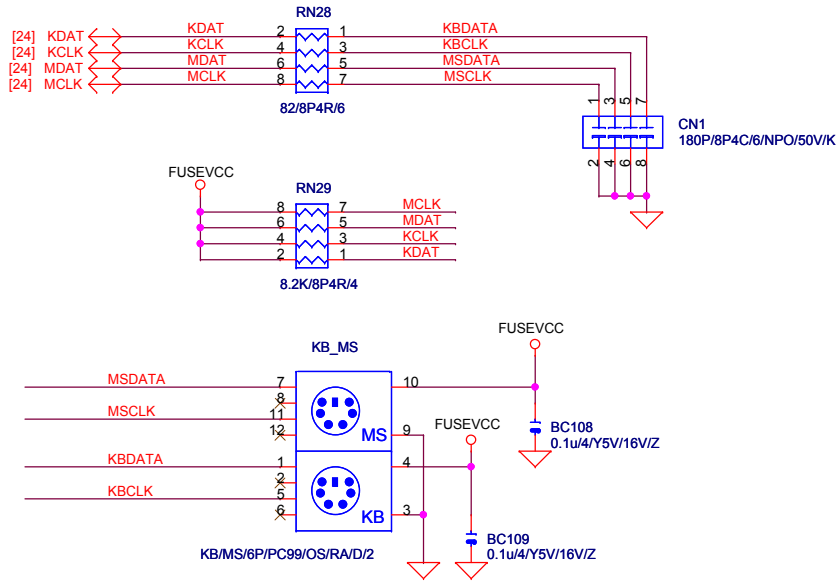


CASE OPEN

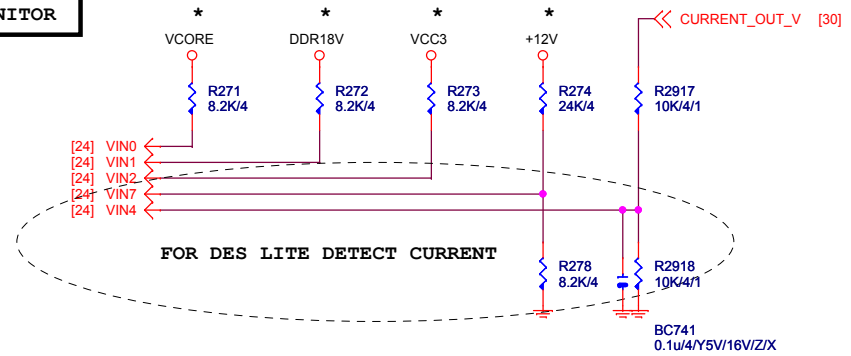


Case Open Circuits

KB/MS

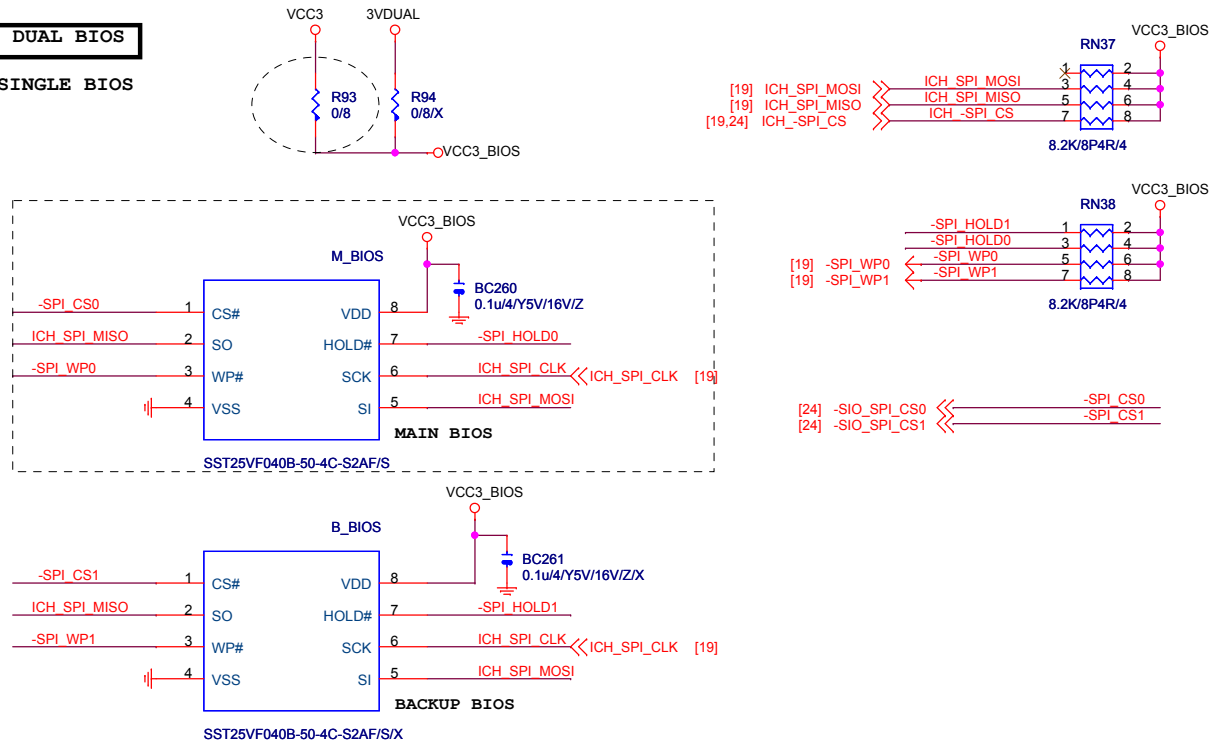


VOLTAGE-- H/W MONITOR



DUAL BIOS

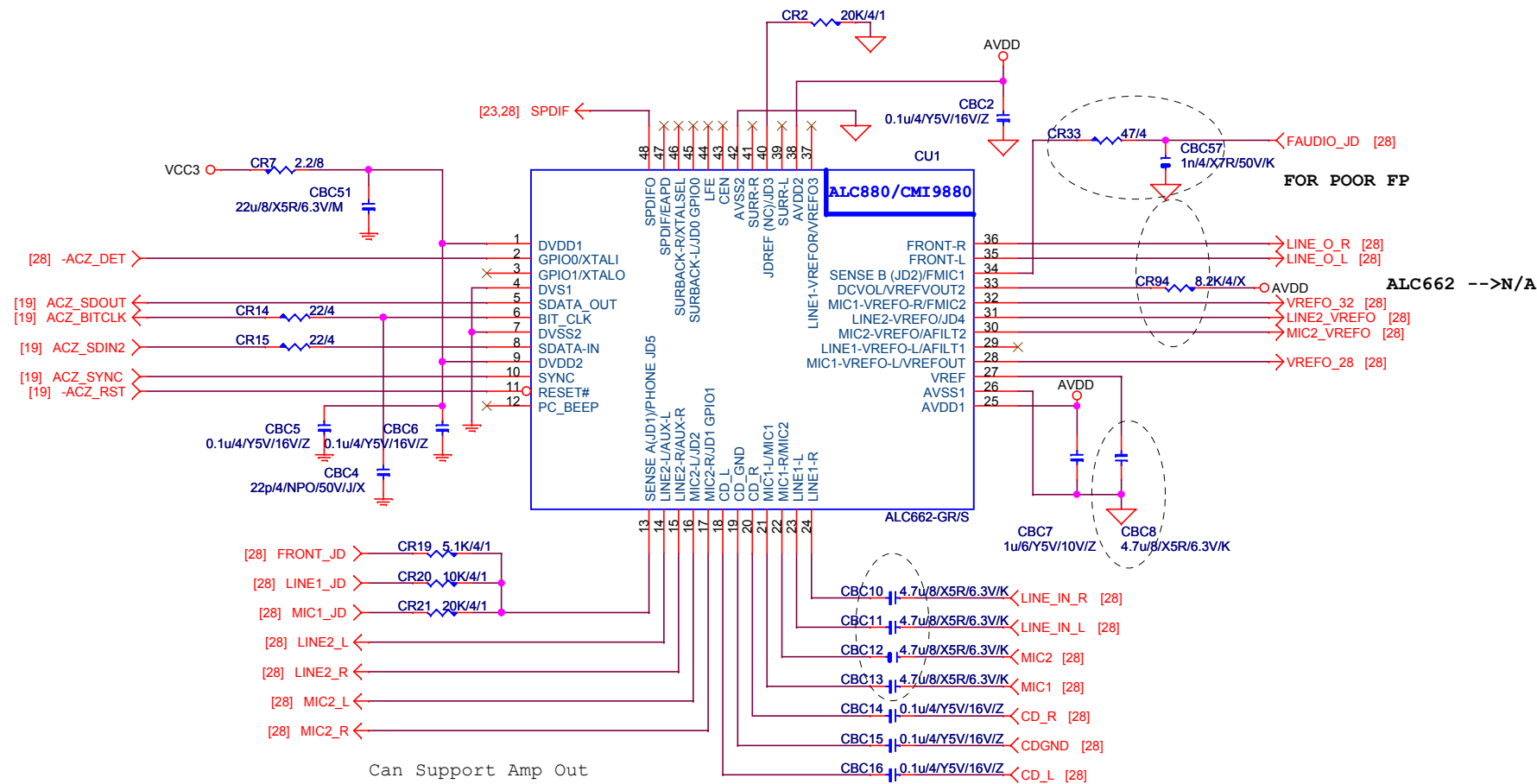
SINGLE BIOS



Gigabyte Technology

Title			HW-MONITOR/CI/KB/MS/BIOS	
Size	Custom	Document Number	GA-G31M-S2C	
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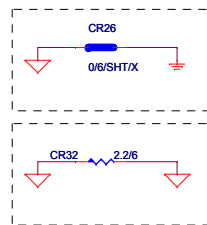
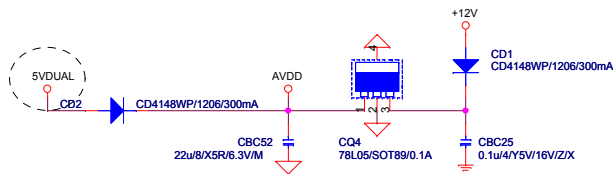
Rev 1.11



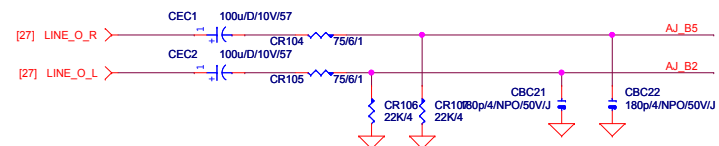
Gigabyte Technology

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Size	Document Number	Rev
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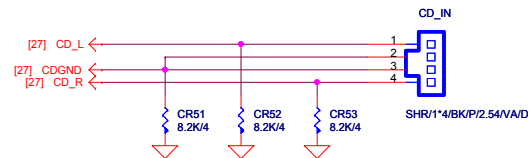
CODEC POWER/EMI PAD



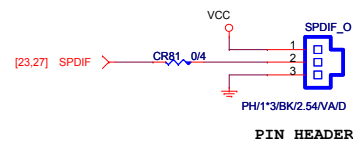
LINE-OUT



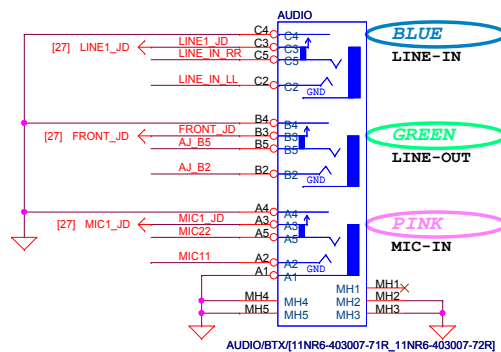
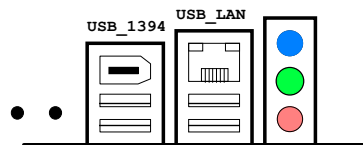
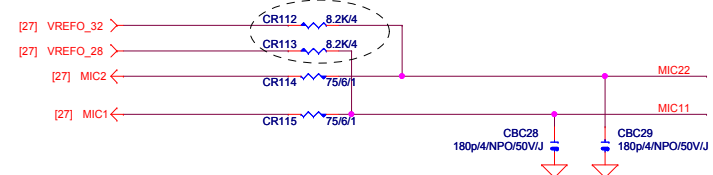
CD	IN
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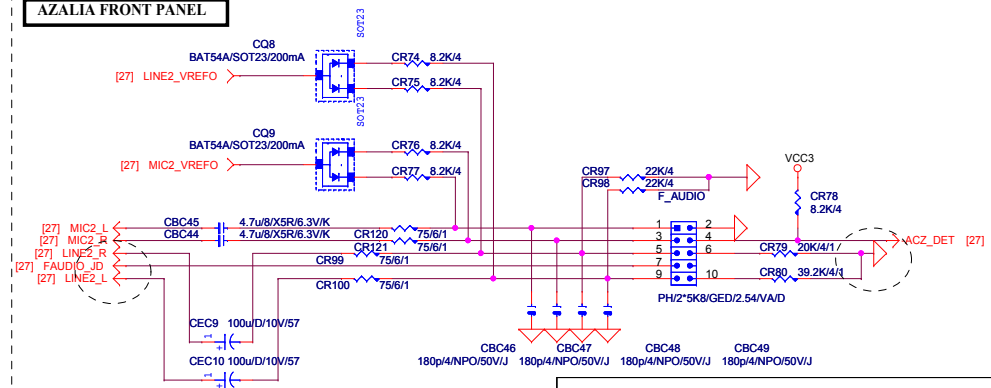
SPDIF IN



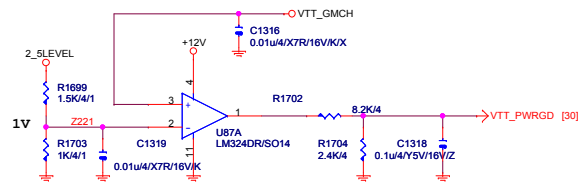
AZALIA JACK

**MIC-IN**

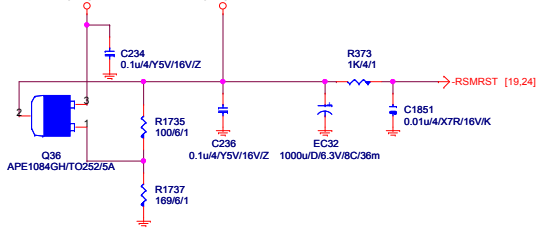
AZALIA FRONT PANEL



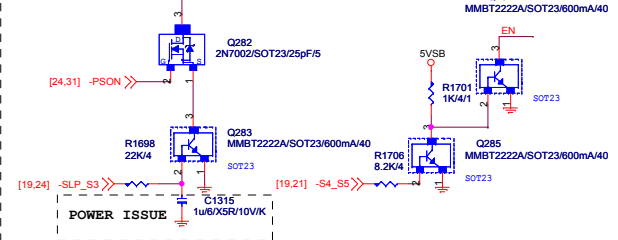
VTT_PWRGD



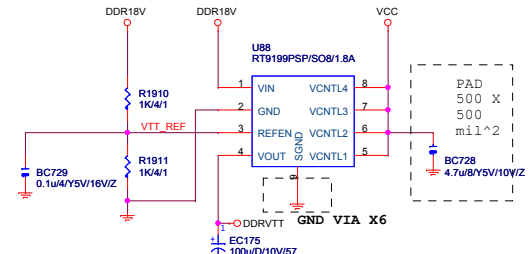
3VDUAL



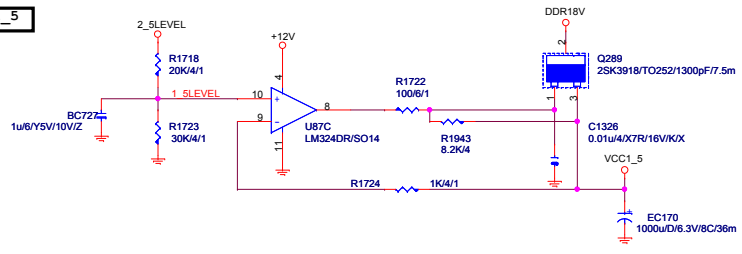
PWR_SEQ



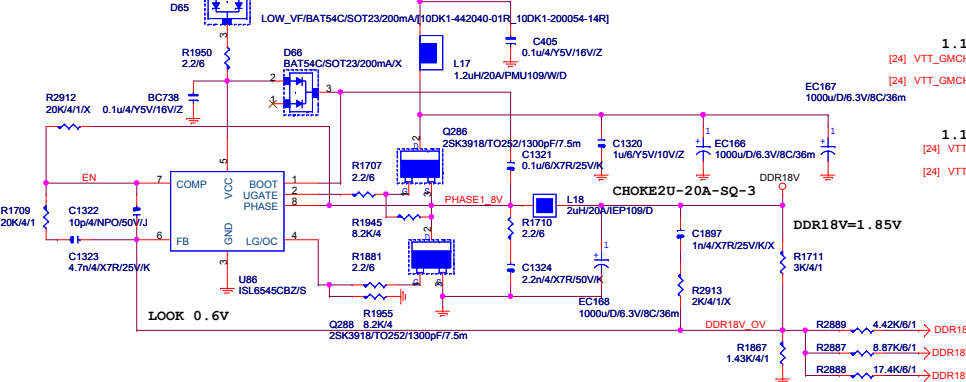
DDR_VTT



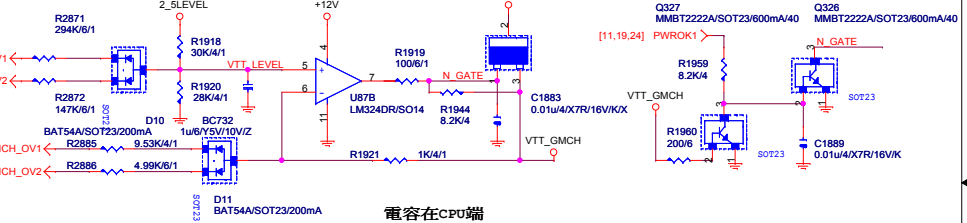
VCC1_5



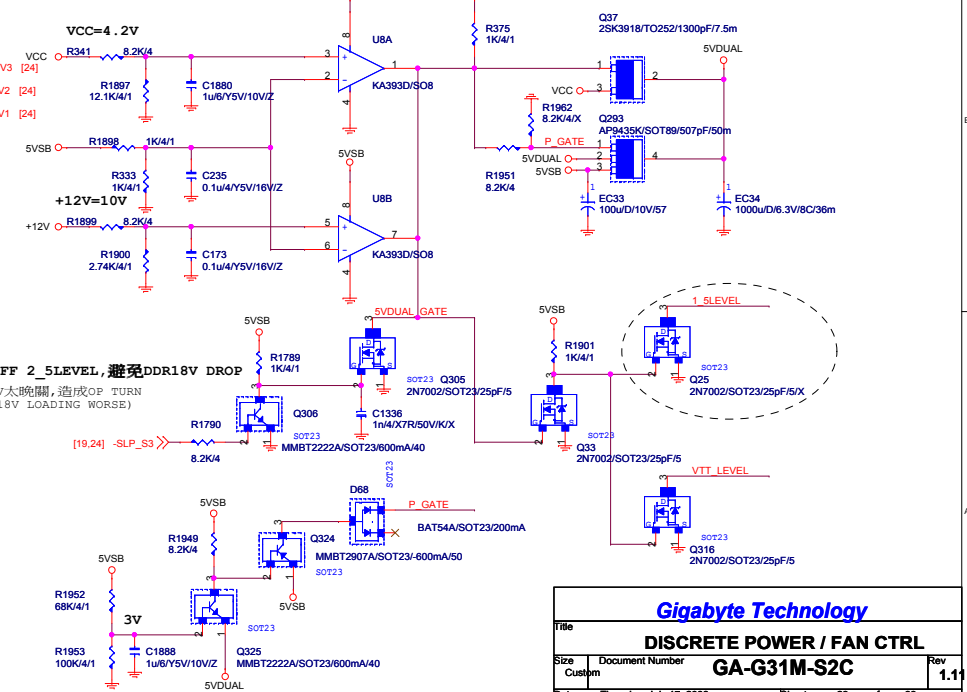
DDR18V



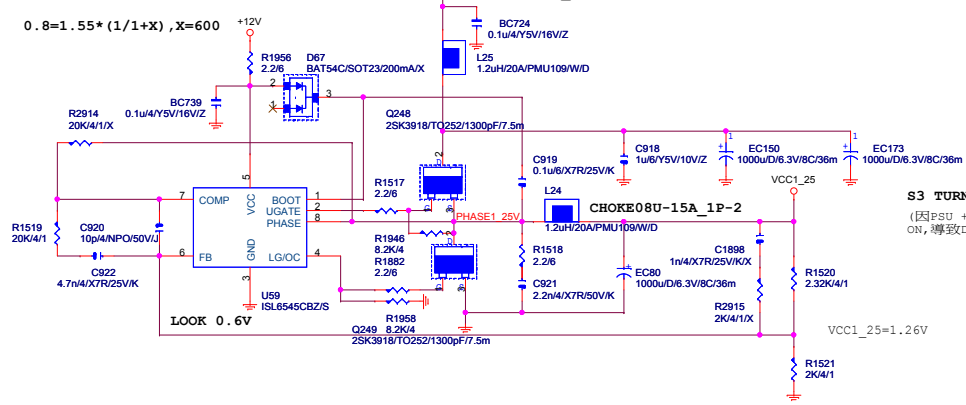
VTT_GMCH



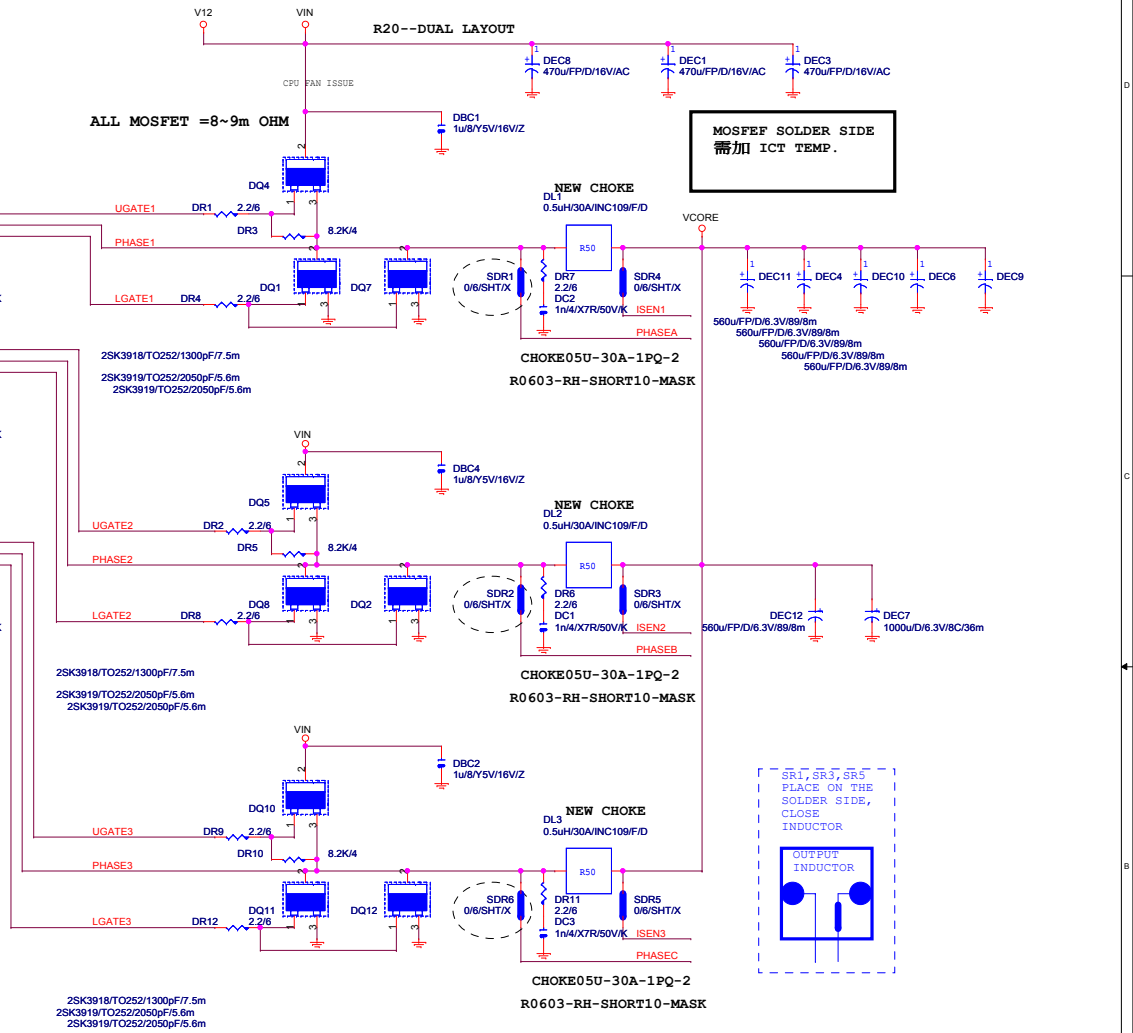
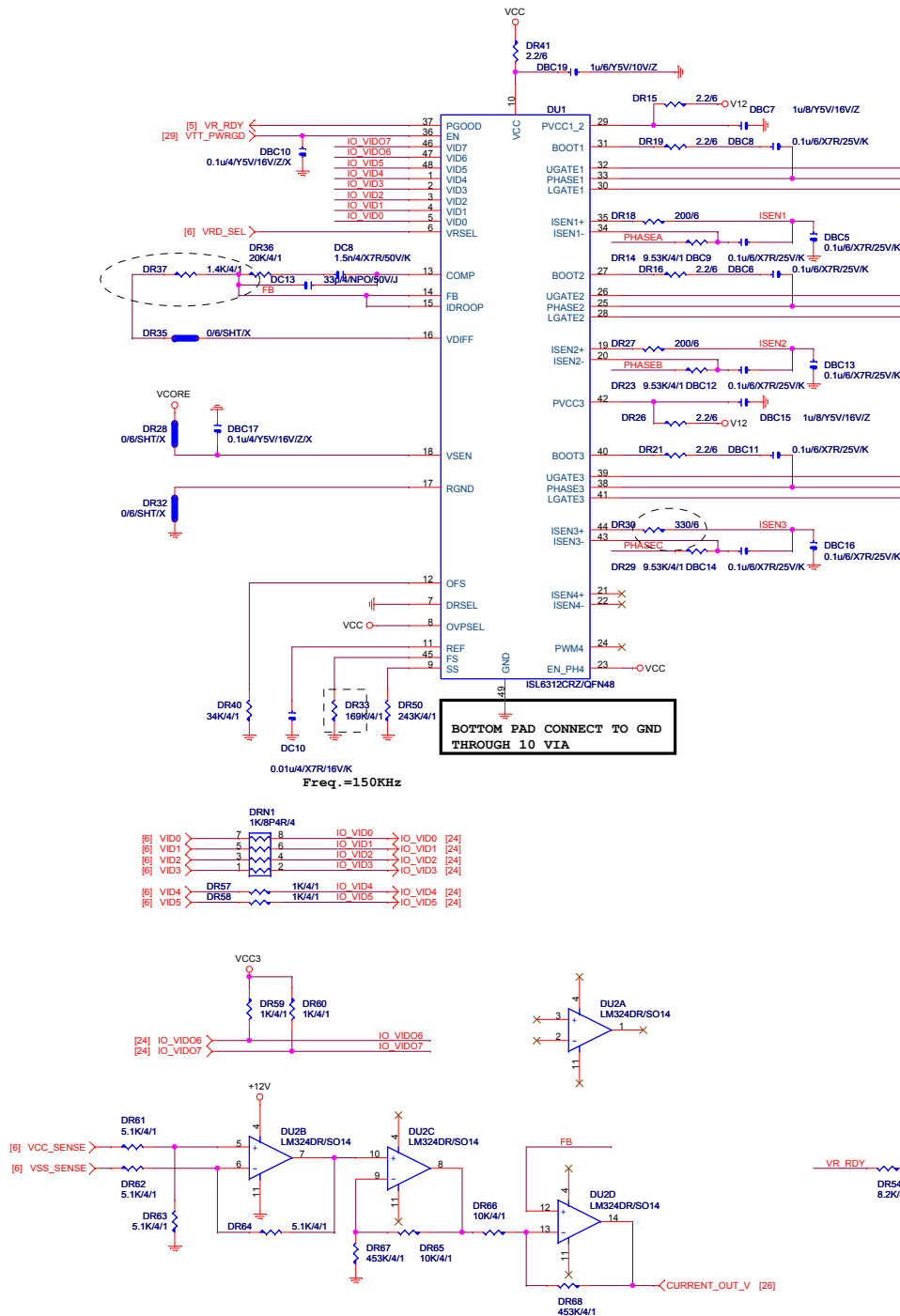
5VDUAL



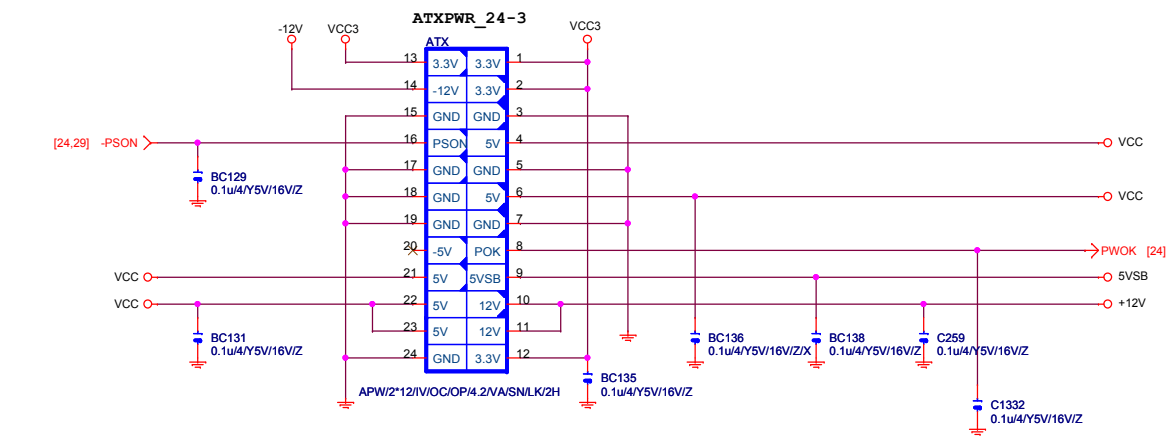
VCC1_25



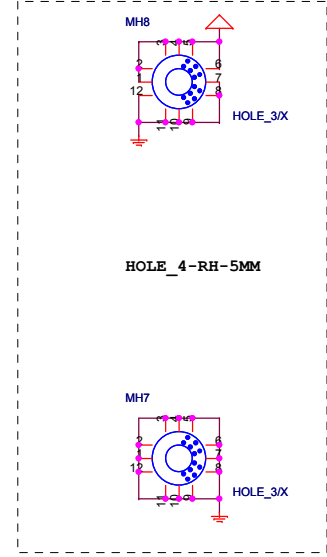
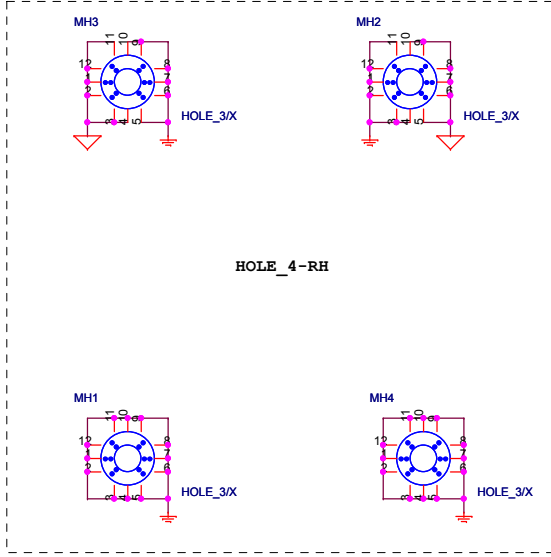
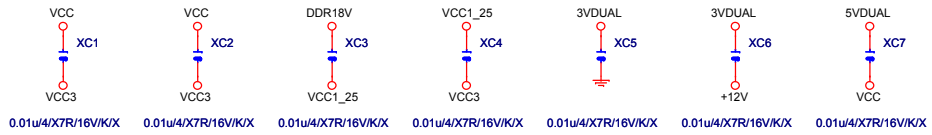
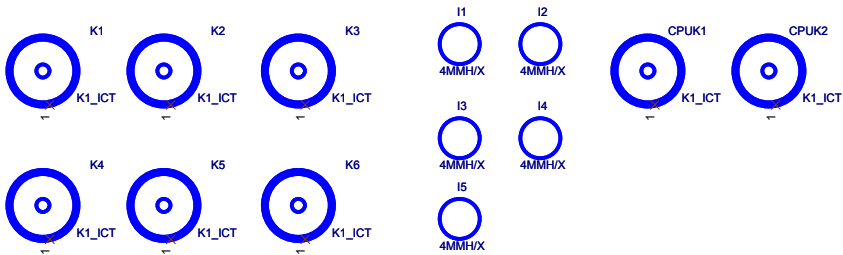
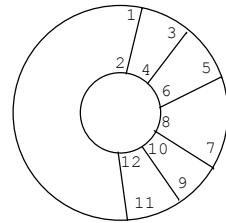
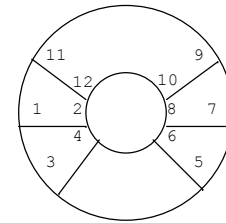
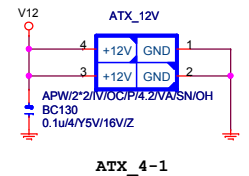
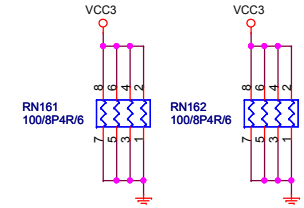
S3 TURN OFF 2_5LEVEL, 避免DDR18V DROP
(因PSU +12V太晚關, 造成OP TURN ON, 導致DDR18V LOADING WORSE)



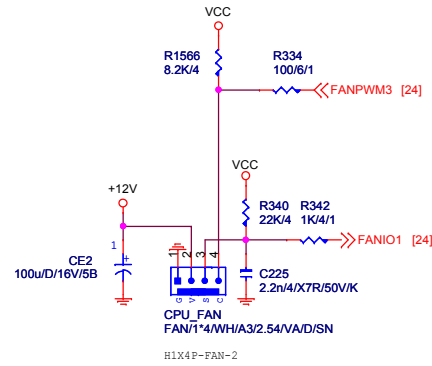
ATX POWER CONNECTOR



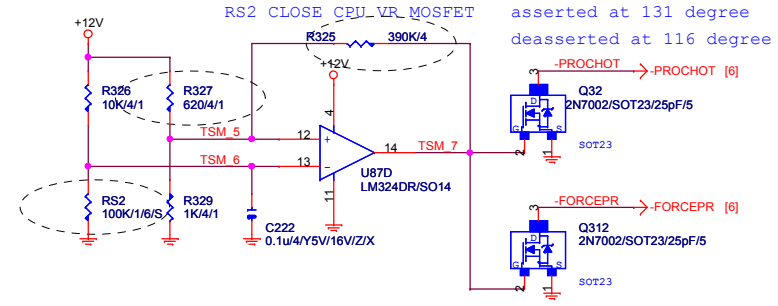
FIX PWR AcBel (ATX-400C-A2ADB)



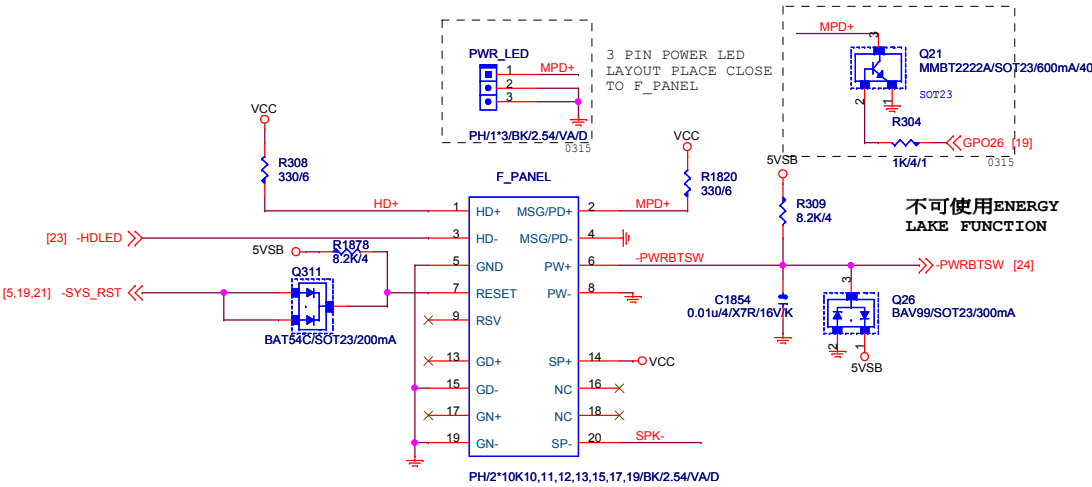
CPU SMART FAN SMART FAN



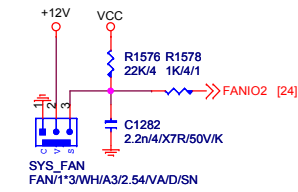
PROCESSOR HOT



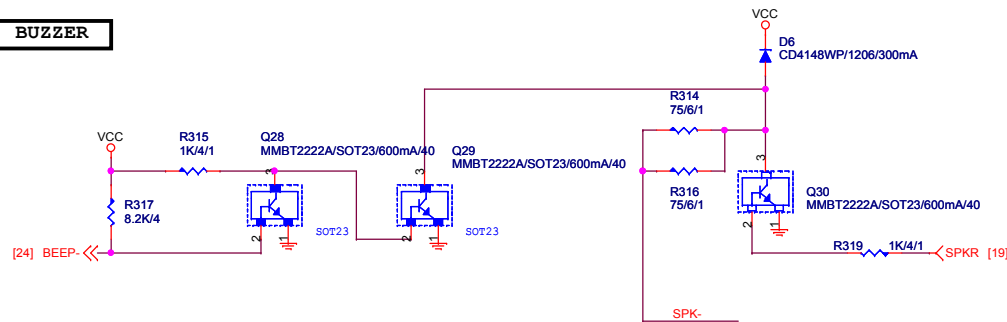
INTEL FRONT PANEL



SYS_FAN



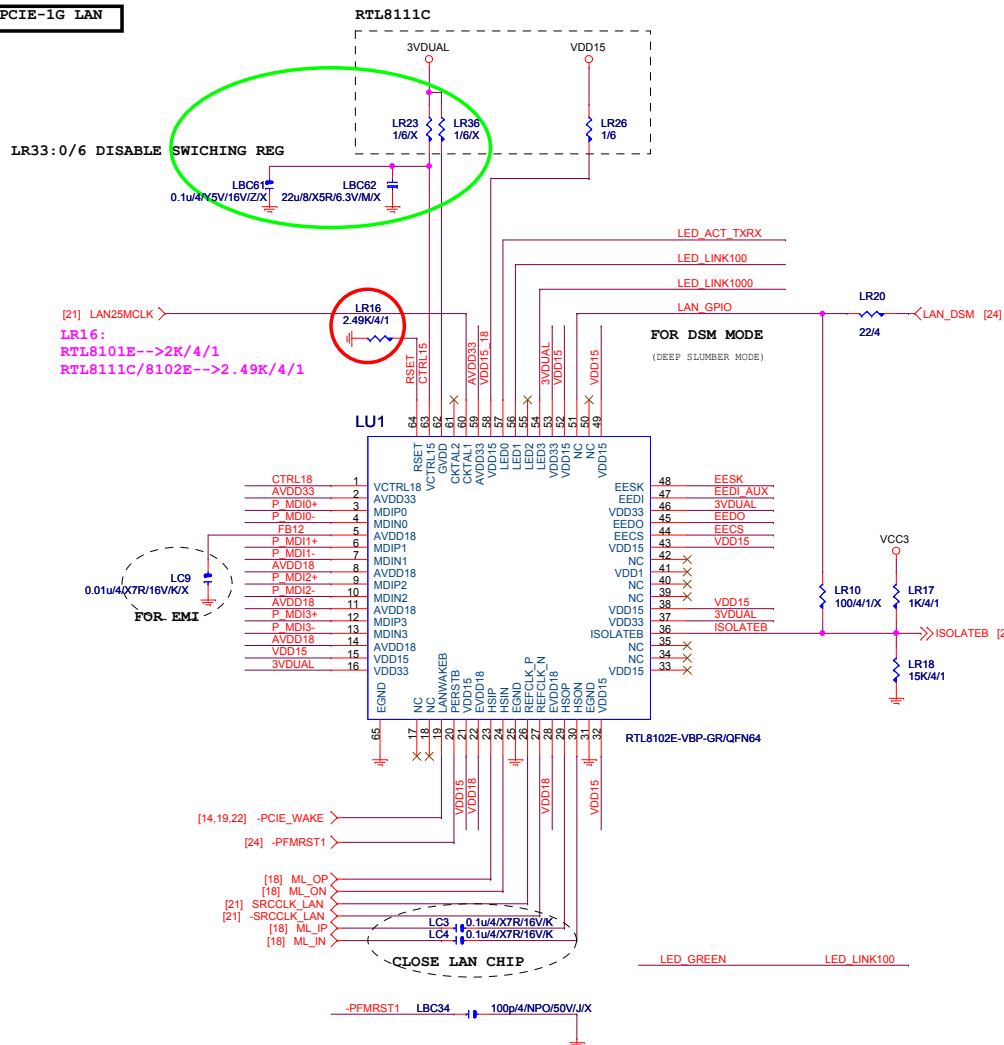
BUZZER



Gigabyte Technology

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PCIE-1G LAN

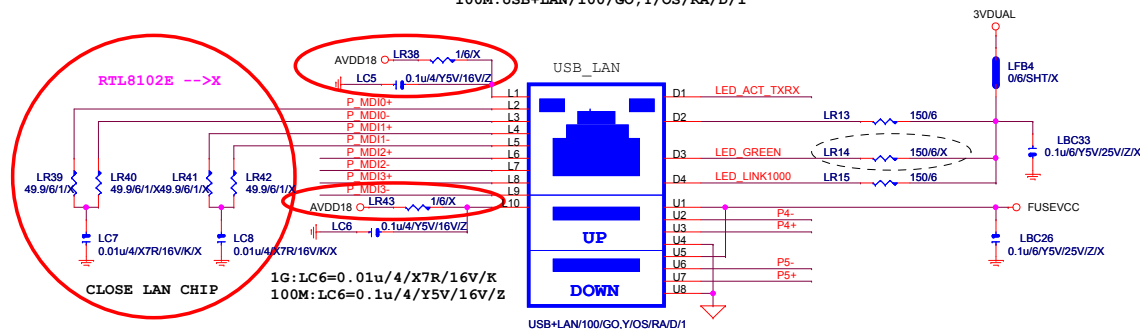


USB_LAN CONNECTOR

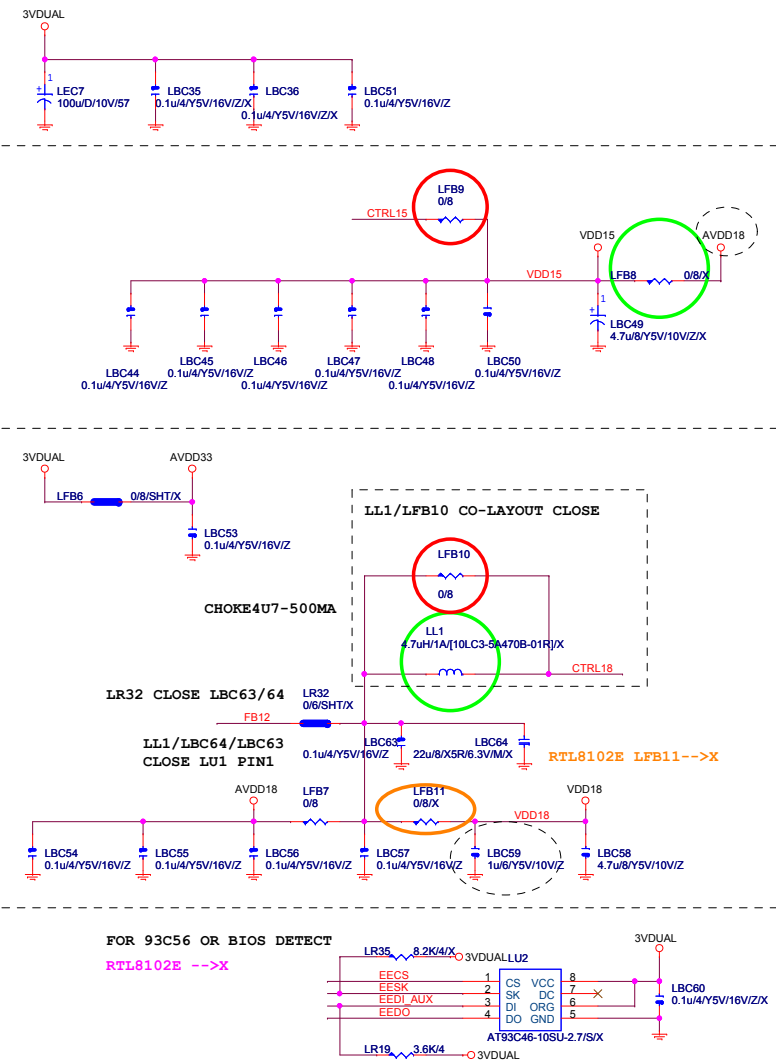
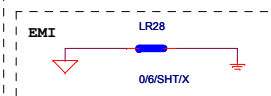
```
RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8102E:LC5/LC6-->O
RTL8111C:LC6-->O
```

```
RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)
```

```
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1
```



USB LAN



Gigabyte Technology

REALTEK RTL8111C/8101E

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